DINI GROUP

LOGIC Emulation Source

# User Manual
# DNMEG_V6HXT

LOGIC EMULATION SOURCE

# DNMEG_V6HXT User Manual Version 2.0

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Chapter 1

# Introduction

*This User Manual accompanies the DNMEG_V6HXT Logic Emulation Board. For specific information regarding the Xilinx Virtex-6 parts, please reference the datasheet on the Xilinx website.*

## 1 DNMEG_V6HXT LOGIC Emulation Kit

**Overview**

The **DNMEG_V6HXT** is a complete network interface solution featuring high speed serial IOs. The **DNMEG_V6HXT** can be used stand-alone, without hosting (contact factory for chassis options if required) hosted by 8-lane PCIe cable (GEN1/GEN2) plugged into ASIC Prototyping boards from the DINI product line as an expansion peripheral. FPGA configuration and other miscellaneous board functions are controlled by the NXP LPC1754 ARM based microcontroller, including the front panel LCD.

A single **DNMEG_V6HXT** configured with the Xilinx Virtex-6, XC6VHXT565T FPGA, can emulate up to 4 million gates of logic as measured by a reasonable ASIC gate counting standard. This gate count estimate number does not include embedded memories and multipliers resident in each FPGA. One hundred percent (100%) of the FPGA resources are available to the user application, but the user's application must include all necessary MACs and the PCIe Bridge. The **DNMEG_V6HXT** achieves high gate density and allows for fast target clock frequencies by utilizing FPGAs from Xilinx's 40nm Virtex-6 HXT family.

**Virtex-6 HXT FPGAs from Xilinx**

The **DNMEG_V6HXT** is configured with a Xilinx Virtex-6, HXT family FPGA, in the FFG1923 package. This package supports 720 IOs and all are utilized. The HXT FPGAs contain high-speed transceiver PHYs of two different types. GTX transceivers are capable of handling data rates of 150 MB/s to 6.5 Gb/s, making these useful for lower speed Ethernet, Serial ATA, and GEN1/GEN2 PCI Express. The GTH transceivers are tuned higher, 2.48 to 11.18 Gb/s, making them applicable to 10 gigabit Ethernet (10 GbE). Two possible FPGAs can be stuffed: XC6VHX380T or the

XC6VHX565T. The XC6VHX380T comes in three speeds grades, with -3 being the fastest. The larger XC6VHX565T is limited to the -2 speed grade. This means the smaller device can be clocked at a higher frequency at the cost of slightly fewer FPGA logic resources. The XC6VHX565T is capable of handling >4M ASIC gates of logic and is among the largest of the FPGAs shipping from any vendor in 2011. Features of the Virtex-6 HXT FPGAs include the efficient, dual-register 6-input look-up table (LUT) logic, 18 Kb (2 x 9 Kb) block RAMs and second generation DSP48E1 slices (includes 25 x 18 multipliers). Floating point functions can be implemented using these DSP slices.

**Network Prototyping with FPGAs at the High End**

**40GbE/100GbE with CFP Module**
The **DNMEG_V6HXT** hosts a single **C Form-factor pluggable** (CFP) module that is connected to 10-lanes of GTH transceivers. A variety of CFP MSA fiber optic transceiver modules (not supplied) are compatible to this connector and provide PHYS for 40Gb/s and 100Gb/s applications. The user is required to provide the MAC IP for the FPGA.

**40GbE with QSFP+**
The **DNMEG_V6HXT** has two **Quad Small Form Factor Pluggable** (QSFP+) connectors. Each QSFP+ is attached to 4-lanes of GTH transceivers. A variety of QSFP+ PHYS can be used here, creating a single lane of 40GbE, or 4-lanes of 10GbE. The user is required to provide the MAC IP for the FPGA.

**10GbE with SFP+**
The **DNMEG_V6HXT** has four **Small Form Factor Pluggable** (SFP+) connectors, each attached to single GTH lane. Again, a variety of SFP+ PHYS can be used here, with the most popular being 10GbE.

**10/100/1000 BaseT with SFP** Eight SFP connectors are attached to single GTX lane. A variety of SFP PHYS can be used here, with the most popular being 1000BaseT.

**Two Serial-ATA Ports (SATA II)**
The FPGA has dual SATA II (Serial ATA II) connectors attached to GTX. With SATA IP integrated into the FPGA logic, SATA cables connected can provide additional high-speed data paths to off board peripheral.

**GTX Expansion Header**
Eight lanes of GTX are connected to our standard GTX expansion header (purple thing in block diagram). Daughter cards such as the DNSEAM_SFP can be used here to add 8 SFP sockets, potentially adding 1x/2x/4x Fibre Channel, 10/100/1000GbE Ethernet, XAUI, SATA or Serial RapidI/O to the mix.

All or any subset of the above interfaces high speed serial interfaces can be used simultaneously. Two GTH channels are connected to high-speed SMAs.

### DDR3 - Bulk Memory

A single PC3-8500 DDR3 UDIMM socket enables up to 16GB (plus ECC) of memory for bulk storage and lookup. With a 16GB UDIMM memory stick, the configuration is 2048M x 72. Using a -2 or -3 speed grade FPGA, this interface is tested at the maximum FPGA IO frequency: 533 MHz (1066 Mb/s with DDR). You are welcome to use this memory as 64-bits with 8 bits of error correction (ECC), or as a 72-bit memory without correction.

This is the same UDIMM interface used in our blockbuster DNPCIe_10G_HXT_LL product. To minimize data synchronization across clock boundaries, important for networking applications, it probably makes sense to clock this DDR3 interface at a 3x multiple of the base Ethernet frequency of 156.25 MHz, which is 468.75 MHz. A 3x phase synchronous clock can be easily generated internal to the FPGA, allowing zero latency synchronous data transfers between the Ethernet packet receiving logic and the DDR3 memory controller. The DDR3 controller can be optimized in any way you choose. Dini Group provide several Verilog examples, at no charge. All functions of the DDR3 DRAM can be exploited and optimized. Up to 8 banks can be open at once. Timing variables such as CAS latency and precharge can be tailored to the minimum given your operating frequency and the timing specification of the exact DDR3 memory utilized.

Alternate UDIMM memories are in development, including an RLDRAM and a QDRII+ option.

### Daughter cards for customization and expansion: MEG-Array and FMC

### MEG-Array

Two 400-pin FCI MEG-Array connectors are attached to a single interface on the FPGA. One MEG-Array connector is on the top and one the bottom. The signals are shared. The bottom connector is used when this card is designated as a peripheral to our ASIC prototyping product. The top connector is used when this card is used stand-alone and application of one of our many DNMEG daughter cards is useful. This is a non-proprietary, industry standard connector and the mating connector is readily available. Dini Group can provide the mating connector at cost custom User daughter cards. The 192 signals (96 pairs) to/from each of these MEG-Array expansion connectors are routed differentially and can run at the limit of the Virtex-6 FPGA IOs: 710 MHz. Clocks, resets, and presence detection, along with abundant (fused) power are included in each connector.

### FMC (Vita-57)

FPGA Mezzanine Card, or FMC, as defined in VITA 57, provides a specification describing an IO mezzanine module with connection to an FPGA or other device with reconfigurable IO capability. Most vendors of FMC daughter cards tend to ignore the specification, making this interface standard a questionable option. Also, the total

number of IOs in the specification is much too small. But there are some good A/D and D/A cards that adhere enough to the specification to be useful.

**Easy Configuration via PCIe, USB, or Ethernet**
Configuration of the FPGAs is under the control of an embedded CPU, an ARM-based LPC1754 from NXP. Xilinx is not nice enough to supply a serial PROM large enough to configure the XC6VHXT565T, so we need to use rather exotic methods to create enough onboard EEPROM storage for this function.

**Status LEDs, Debug**
As with all of our ASIC emulation boards, the **DNMEG_V6HXT** is loaded with LEDs. The LEDs are stuffed in several different colors (red, green, blue, orange et al.). Blinking these LEDs in a controlled fashion can confuse a trout. While this is unlikely to be fatal to the little fish, make sure an adult is present and wear eye protection when testing this feature. These LEDs are user controllable from the FPGAs so can be used as visual feedback in addition to the task of distracting fish. A JTAG connector provides an interface to ChipScope, Veridae, and other third party debug tools.

# 2 DNMEG_V6HXT Logic Emulation Board Features

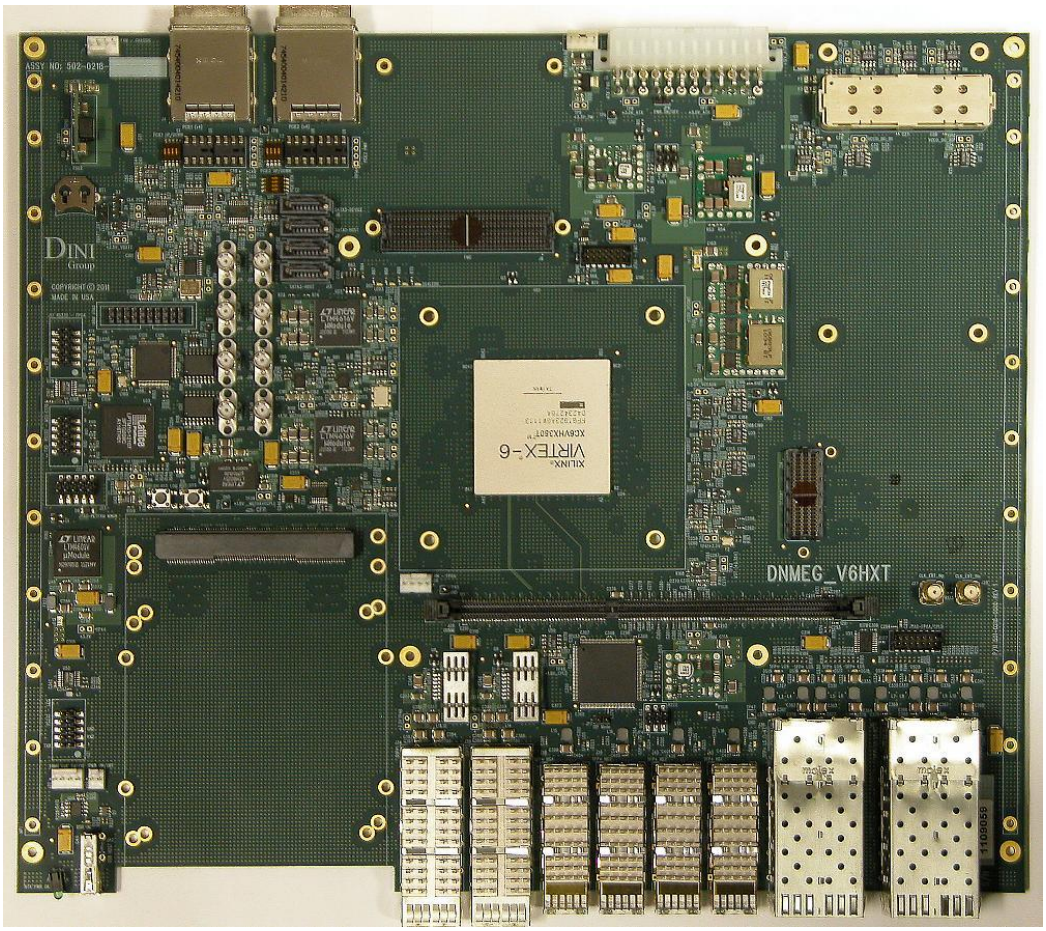



Figure 1 - DNMEG_V6HXT Logic Emulation Board

- Stand-alone or hosted via PCI Express Cable (GEN1/GEN2)
- Xilinx Virtex-6 FPGA (FF1760), populated with any of the following options:
  - XC6VHX380T, -3, -2, -1 (fastest to slowest)
  - XC6VHX565T, -2, -1
- GTX Transceiver Interfaces (up to 6.6Gbps)
  - Dual PCI Express Cable (x4)
  - Eight SFP+ (x1)
  - Dual SATA II (x1) – Host/Device
  - FMC (x10) – Daughter Card (HPC)

  - SEARAY (x8) – GTH Expansion Header
- GTH Transceiver Interfaces (2.488Gbps to 11Gbps)
  - CFP (x10)
  - Dual QSFP+ (x4)
  - Four SFP+ (x1)
  - SMA (x2) – Shares a CFP QUAD Tile
- FPGA Configuration
  - Configuration Options - USB, PCI Express, JTAG
  - Stand-alone configuration with USB Flash Drive
  - Encryption, Readback and Partial Reconfiguration
- Flexible Clock Resources
  - FPGA Clock Generator - Si5338
    - CFP Clock Network (CML)
    - QSFP Clock Network (LVPECL)
    - SFP+ HS/LS Clock Network (LVPECL)
  - PCI Express Clock (100MHz)
  - External Clock (LVDS) Input via SMA (x2)
  - Multiple clocks from the Daughter Card Header
  - Fixed Oscillator for SATA II (150MHz)
  - Clock Test Points (x2)
- Memory
  - DDR3 SDRAM UDIMM, 8GB (1G x 72), 240 pin SODIMM (PC3-8500)
  - Serial EEPROM, 64Kb (8192 x 8)
- Daughter Card Headers (LVDS) – MEG-Array (400 pin)
  - 96 LVDS unidirectional pairs + clocks (or 192 single-ended)
  - 550 MHz on all signals with source synchronous LVDS
  - Signal voltage set by daughter card (+1.2V to +2.5V)
  - +12V (24W max) and +3.3V (10W max), Supplied power rails (fused)
- LCD Display (192 x 64 pixel)
- User LED's

- Onboard Distributed Power Supplies
- Full support for Embedded Logic Analyzers
    - ChipScope Logic Analyzer
- Dual RS232 Port for Microcontroller and FPGA - 10 pin Header
- Stand Alone operation, requires an external +12V ATX power supply with a ATX Power Connector.

# 3 Package Contents:

Before using the kit or installing the software, be sure to check the contents of the kit and inspect the board to verify that you received all of the items. If any of these items are missing, contact Dini Group before you proceed. The DNMEG_V6HXT Logic Emulation Board kit includes the following:

- USB Flash Drive (4GB) – USB007, P/N UFDCR-4096
- UDIMM DDR3 4GB (PC3-10600), 240 Pin, Crucial, P/N CT51272BA1339
- Active Cooler for 2U Server & Up – Dynatron, P/N K555 or,

- Passive Heatsink for 1U Server – Dynatron, P/N K1

- Cable (RS232), DB9 Female to DB9 Female, 6ft – Jameco, P/N 132346
- Cable Straight, IDC 10-Pin Socket to DB9 Male, 18" – PCH Cables, P/N 000-F903-N
- Customer Support Package (on USB Flash Drive)
    - Documentation (Datasheets, User Manual and Schematics)

- FPGA Reference Designs (Verilog)
- Host Software (AETest)

Optional items that support development efforts (not provided):

- ✓ Xilinx ISE Software
- ✓ Xilinx Platform Cable USB
- ✓ LCD Display, 192 x 64 pixel FFSTN Grey/White – Matrix Orbital P/N GLK19264-7T-1U-FGW

- ✓ Cable Crossed, IDC 10-Pin Socket to DB9 Male, 18" – PCH Cables, P/N 000-F903 (used to connect the LCD to the DNMEG_V6HXT board)
- ✓ Additional DDR3 SDRAM UDIMMs (Available upon request)

# 4 Inspect the Board

Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment. Verify that all components are on the board and appear intact.

# 5 Additional Information

For additional information, please visit http://www.dinigroup.com/. The following table lists some of the resources you can access from this website. You can also directly access these resources using the provided URLs.

| Resource | Description/URL |
|---|---|
| User Manual | This is the main source of technical information. The manual should contain most of the answers to your questions |
| Demonstration Videos | MEG-Array Daughter Card header insertion and removal video |
| Dini Group | The web page will contain the latest user manual, application notes, |

| Resource | Description/URL |
|---|---|
| Web Site | FAQ, articles, and any device errata and manual addenda. Please visit and bookmark: http://www.dinigroup.com |
| Data Book | Pages from Virtex-6 Databook, which contains device-specific information on Xilinx device characteristics |
| E-Mail | You may direct questions and feedback to Dini Group using this e-mail address: support@dinigroup.com |
| Phone Support | Call us at **858.454.3419** during the hours of 8:00am to 5:00pm Pacific Time. |
| FAQ | The download section of the web page may contain a document called **MEG_V6HXT Frequently Asked Questions (FAQ)**. This document is periodically updated with information that may not be in the User's Manual. |

Chapter 2

# Getting Started

*Congratulations on your purchase of the DNMEG_V6HXT Logic Emulation Board. The remainder of this chapter describes how to start using the DNMEG_V6HXT Logic Emulation Board.*

## 1 Before You Begin

### 1.1 Configuring the Programmable Components

The DNMEG_V6HXT has been factory tested and pre-programmed to ensure correct operation. The user does not need to alter any jumpers or program anything to see the board work.

### 1.2 Warnings

- **Test Headers (Over Voltage)** - The test headers are **NOT** 3.3V tolerant. These signals connect directly with the FPGA IO. Take care when handling the board to avoid touching the components and daughter card connections due to ESD.

- **Mechanical Stress** – Board stiffeners are provided to reduce mechanical stress; however, inserting and removing Daughter Cards may add additional stress that may cause board failures.

- **ESD Warning** - The board is sensitive to static electricity, so treat the PCB accordingly. The target markets for this product are engineers that are familiar with FPGAs and circuit boards. However, if needed, the following web page has an excellent tutorial on the "Fundamentals of ESD" for those of you who are new to ESD sensitive products:

  http://en.wikipedia.org/wiki/Electrostatic_discharge

### 1.3 Exploring the Customer Support Package

The USB Flash Drive contains the following items, see Figure 2:

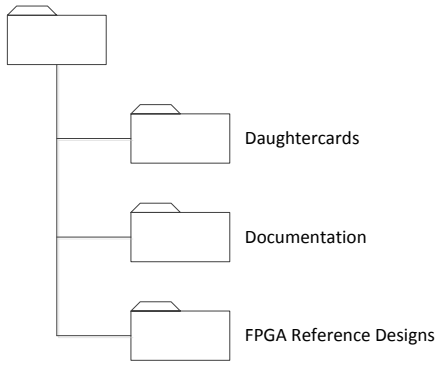



Figure 2 - USB Flash Drive Directory Structure

A description of the USB Flash Drive directory contents is listed in Table 1. Please visit the Dini Group website for the most recent revision of these documents.

Table 1 – USB Flash Drive Directory Contents

| USB Flash Drive Directory Contents | |
|---|---|
| **Directory Name** | **Description of Contents** |
| Daughtercards | Contains the documentations for the DNMEG_OBS Test Daughter Card. |
| Documentation | Contains the Datasheets, User Manual and Schematics for the board. |
| FPGA Reference Designs | Contains source and compiled programming files for the DNMEG_V6HXT reference designs. |

# 2 Board Setup

The instructions in this section explain how to install the DNV6_HXT Logic Emulation board. For the purpose of this demonstration, the DNV6_HXT will be configured in Stand-Alone mode connected using the RS232 Interface.

## 2.1 Installing the FPGA Cooler

In order to provide cooling for the FPGA, the kit contains an Active Cooler – Dynatron, P/N K555. To avoid mechanical stress during shipment the part is not installed on the board, please proceed as follows to install the fan/heatsink combo;

### 2.1.1 Tools required

- ESD Safe Assembly Environment
- Phillips Screwdriver

### 2.1.2 Assembly Instructions

For assembly instructions, review the following video;

http://youtu.be/XENSvaGmCdg

## 2.2 Before Powering Up the Board

Before powering up the board, prepare the board as follows:

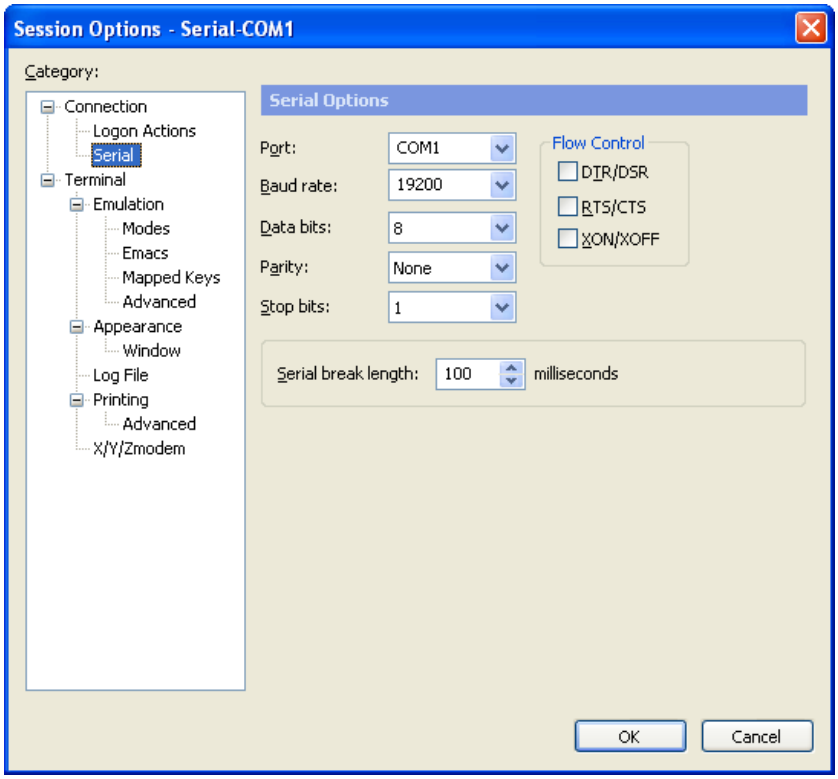
1. If the kit contains a Memory UDIMM module, populate the UDIMM socket. Insert a UDIMM DDR3 SDRAM module into position J29 – P/N CT51272BA1339. Note: Ensure the "VOLT ADJ" jumper (JP4) is set to +1.5V – JP4 pin 1-3.

2. Attach an ATX Power Supply to the "ATX PWR" header (J3).

3. Connect the "RS232 Cable" to the "RS232 - FPGA" header (J17).

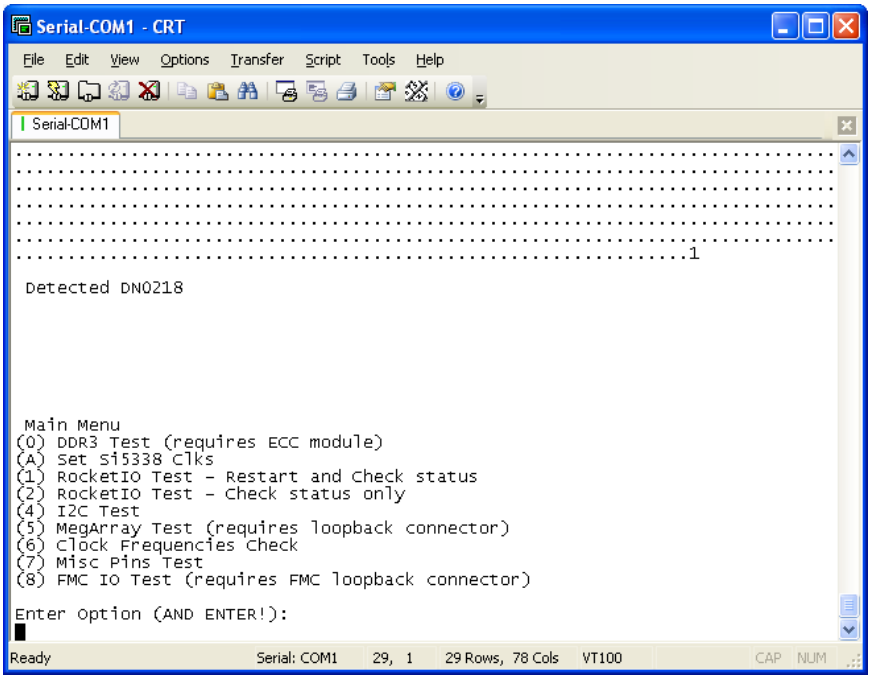
## 2.3 Powering Up the Board

4. Open a Terminal Emulator and configure the session as follows:




5. Power up the board by turning ON the ATX power supply and verify the "ATX PWR OK" LED (DS28) is ON indicating the presence of +12V (located at the bottom-left side of the board).

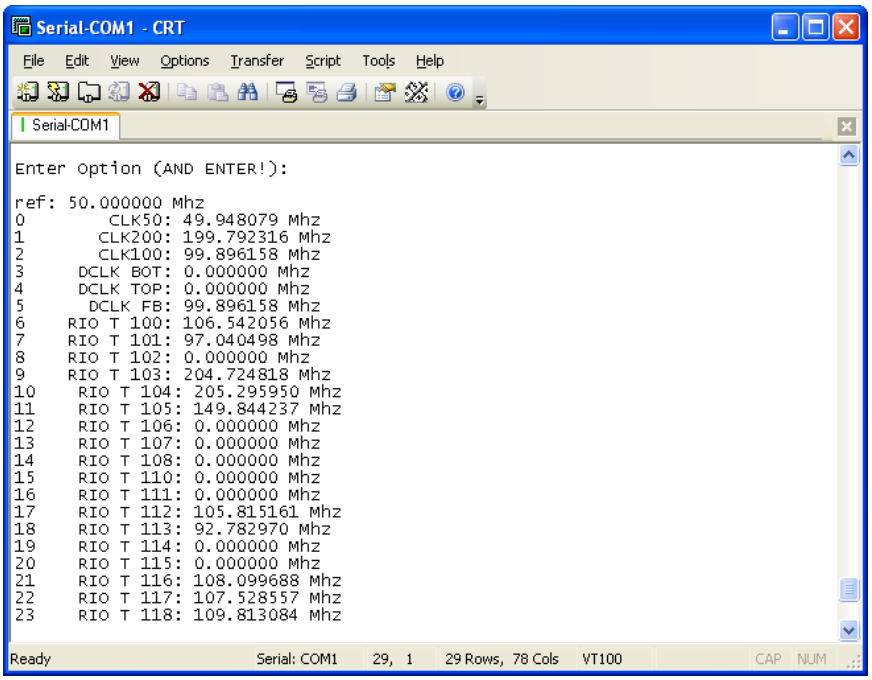
6. Periods will be displayed when the board is powered ON. Verify that the board was correctly identified as a "DN0218" in the terminal window.



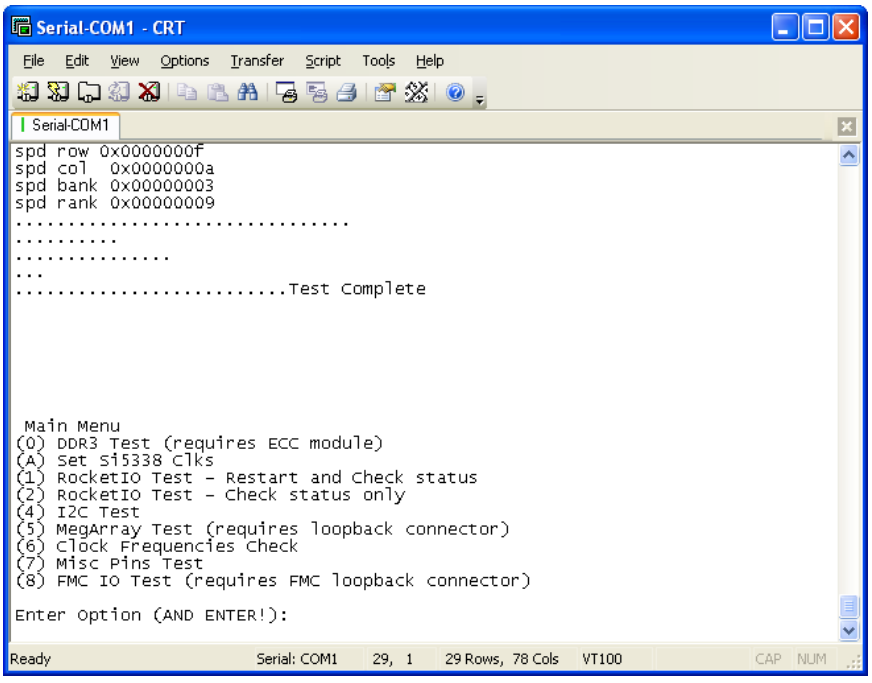

# 3 Using the Reference Design (Main)

This section lists detailed instructions for executing the reference design. Ensure the DNV6_HXT Logic Emulation board is powered ON and a Terminal Window is open to exercise the reference design options;

7. Select test option (6), "Clock Frequencies Check" in the Terminal window and verify that the test displays VALID frequencies.




8. Select test option (0), "DDR3 Test (ECC module required)" in the Terminal window and verify that the test PASS (periods will be displayed as the memory locations are being tested, if no DDR3 Module is present, the test will display read/write errors).


Serial-COM1 - CRT
File Edit View Options Transfer Script Tools Help
Serial-COM1
spd row 0x0000000f
spd col 0x0000000a
spd bank 0x00000003
spd rank 0x00000009
.....Test Complete
Main Menu
(0) DDR3 Test (requires ECC module)
(A) Set Si5338 Clks
(1) RocketIO Test - Restart and Check status
(2) RocketIO Test - Check status only
(4) I2C Test
(5) MegArray Test (requires loopback connector)
(6) Clock Frequencies Check
(7) Misc Pins Test
(8) FMC IO Test (requires FMC loopback connector)
Enter Option (AND ENTER!):
Ready Serial: COM1 29, 1 29 Rows, 78 Cols VT100 CAP NUM

The remainder of the reference design functional tests requires various loop-back test boards/modules to make them PASS, and is not covered in this User Manual. Please reference the Customer Support Package (on USB Flash Drive) for code examples. The next section describes configuring and programming the hardware in detail.

Chapter 3

# Programming/Configuring the Hardware

*This chapter details the programming and configuration instructions for the DNMEG_V6HXT Logic Emulation Board.*

## 1 Introduction

This section of the User Manual presents different methods to configure the Xilinx Virtex-6 FPGA:

- **Configuring the FPGA using USB Flash Drive** – configure the FPGA with a bitfile stored on the USB Flash Drive.
- **Configuring the FPGA using JTAG** – using the Xilinx "Platform Cable USB" and JTAG.

Virtex-6 FPGAs are configured by loading application-specific configuration data - the bitstream - into internal memory. Because the Xilinx FPGA configuration memory is volatile, it must be configured each time it is powered-up. The bitstream is loaded into the device through special configuration pins. These configuration pins serve as the interface for a number of different configuration modes. The following configuration modes are supported:

- Microprocessor-driven SelectMAP configuration mode (x8)
- JTAG/Boundary-Scan configuration mode

The configuration modes are explained in detail in Chapter 2, Configuration Interfaces of the UG360 - Virtex-6 FPGA Configuration User Guide. The specific configuration mode is selected by setting the appropriate level on the dedicated Mode input pins M[2:0].

# 2 Configuring the FPGA using USB Flash Drive

Xilinx does not provide a SPI Flash configuration solution for devices requiring bitstream lengths larger than 128Mb. As a result, a custom configuration solution, using the NXP, LPC1754 32-bit ARM microcontroller and SelectMAP was developed. The user would transfer the bitfile to a USB Flash Drive and the DNMEG_V6HXT will configure the FPGA via SelectMAP (x8). The microcontroller (MCU) provides an USB 2.0 full-speed HOST interface that allows for fast FPGA configuration. Table 2 shows the uncompressed configuration file size for the supported Virtex-6 devices.

Table 2 – Virtex-6 Uncompressed Bitstream Length

| Device | Data Size (Bits) |
|---|---|
| XC6VHX380T | 119,784,608 |
| XC6VHX565T | 160,655,264 |

## 2.1 Setup - Configuring the FPGA using USB Flash Drive

Before configuring the FPGA, ensure the following steps have been completed:

1. Attach an ATX Power Supply to the "ATX PWR" header (J3).

2. Insert a USB Flash Drive in the "USB HOST" connector (J42). Note: Ensure a valid bitfile has been loaded onto the USB Flash Drive.

   - File Format – FAT

   - File Name – fpga_a.bit

## 2.2 Powering Up the Board

3. Power up the board by turning ON the ATX power supply and verify the "ATX PWR OK" LED (DS28) is ON indicating the presence of +12V (located at the bottom-left side of the board).

## 2.3 Configuring the FPGA

Monitor the USB Flash drive LED for a "READ" indication while the MCU reads the bitfile:

4. Verify that the "FPGA_DONE" blue LED (DS5) is enabled, indicating successful configuration of the FPGA from the USB Flash Drive. Note: This process takes approximately 60 seconds to complete.

# 3 Configuring the FPGA using JTAG

This section lists detailed instructions for programming the Xilinx Virtex-6 FPGA using iMPACT, Version 13.1 tools. Before configuring the FPGA, ensure that the Xilinx software and the "Xilinx Platform Cable USB II" driver software are installed on the host computer. The JTAG/Boundary-Scan configuration interface is always available, regardless of the Mode pin settings. The JTAG/Boundary-Scan configuration mode disables all other configuration modes to prevent conflicts between configuration interfaces.

Note: This User Manual will not be updated for every revision of the Xilinx ISE tools, so please be aware of minor differences.

## 3.1 Setup - Configuring the FPGA using JTAG

Before configuring the FPGA, ensure the following steps have been completed:

1. Attach an ATX Power Supply to the "ATX PWR" header (J3).

2. Connect the "Xilinx Platform Cable USB II" to the "JTAG FPGA/CPLD" header (J30).

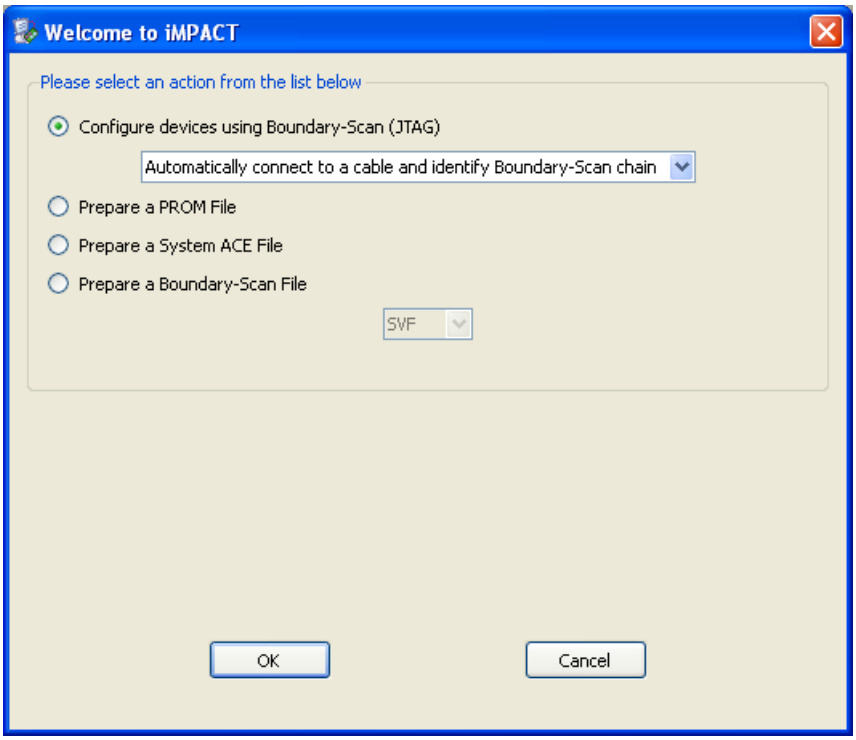
## 3.2 Powering Up the Board

3. Power up the board by turning ON the ATX power supply and verify the "ATX PWR OK" LED (DS28) is ON indicating the presence of +12V (located at the bottom-left side of the board).

## 3.3 Configuring the FPGA

To configure the Xilinx FPGA, perform the following steps:

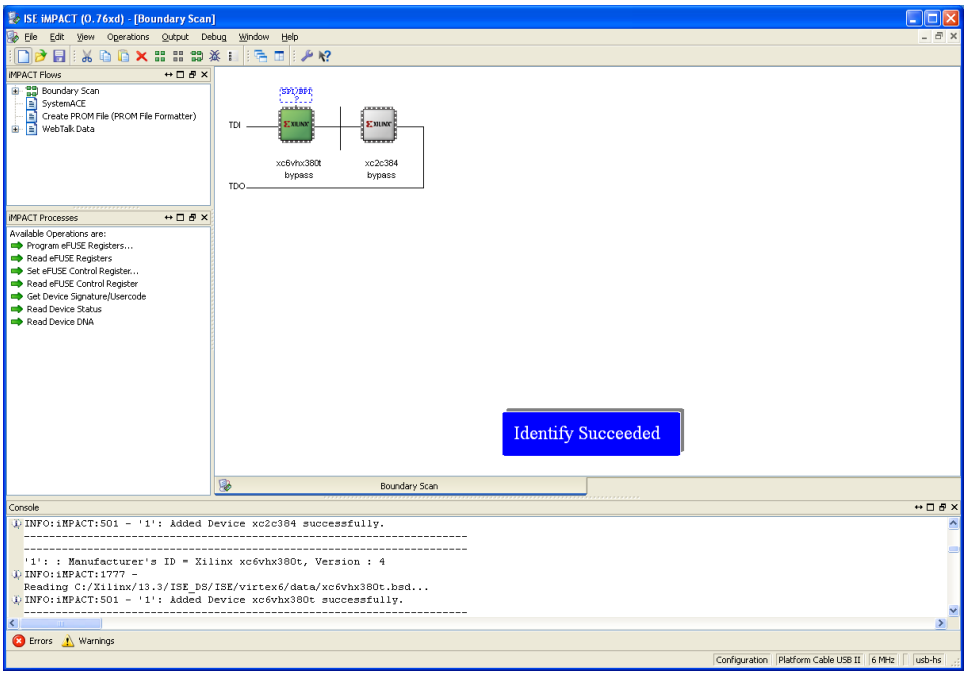
4. Open iMPACT and create a new default project. Select "**Configure devices using Boundary-Scan (JTAG)**" from the iMPACT welcome menu.


Welcome to iMPACT
Please select an action from the list below
Configure devices using Boundary-Scan (JTAG)
Automatically connect to a cable and identify Boundary-Scan chain
Prepare a PROM File
Prepare a System ACE File
Prepare a Boundary-Scan File
SVF
OK
Cancel

5. A pop-up window will display "**Device Programming Properties – Device 1 Programming Properties**". Click "**OK"** to select default options.

6. Right-click on FPGA and select "**Assign New Configuration File**". Specify the location for the FPGA bit file based on the type of FPGA populated e.g. XC6VHX380T; a pop-up window will display "**Attach SPI or BPI PROM**". Click "**NO"** to proceed.

7. Right-click on the FPGA and select the "**Program**" option. Click "**OK**" in the "**Device Programming Properties**" window. A "**Configuration Operation Status**" box will appear indicating programming progress.




8. Verify that the "DONE" blue LED (DS5) is enabled, indicating successful configuration of the FPGA.

Chapter 4

# Hardware Description

*This chapter describes the hardware features of the DNMEG_V6HXT Logic Emulation Board.*

## 1 Description

### 1.1 Overview

The DNMEG_V6HXT is a complete logic prototyping system that enables ASIC or IP designers a vehicle to prototype logic and memory designs for a fraction of the cost of existing solutions. A high level block diagram of the DNMEG_V6HXT Logic Emulation Board is shown in Figure 3, followed by a brief description of each section.

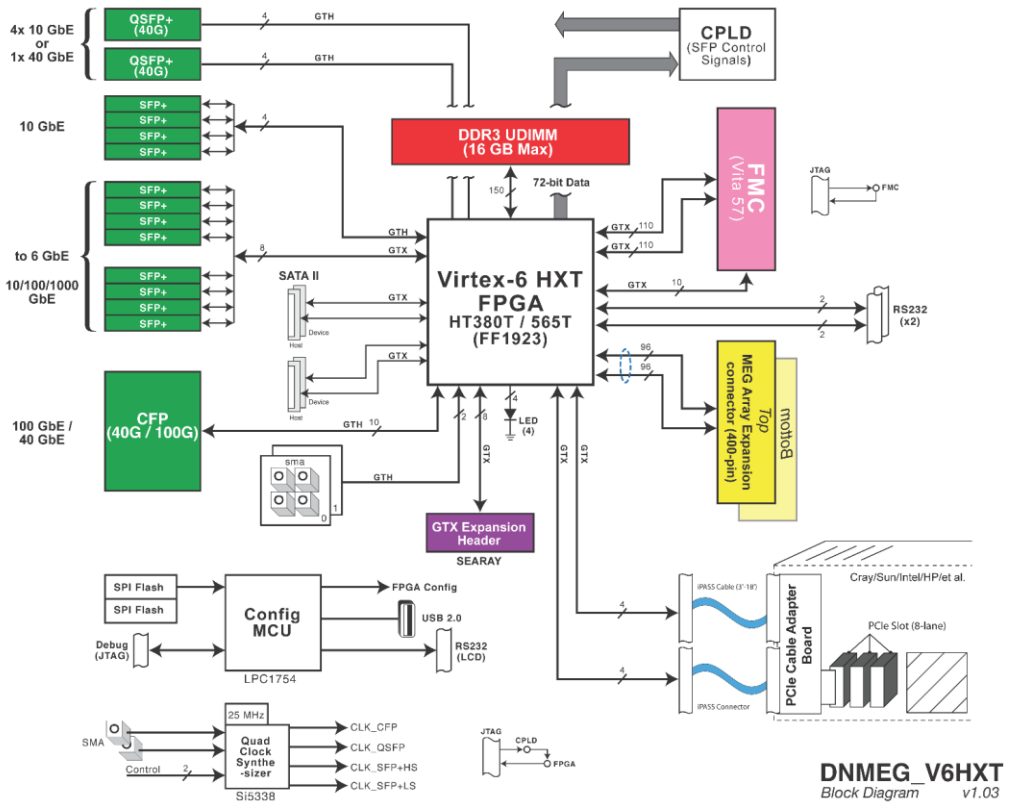



Figure 3 - DNMEG_V6HXT Logic Emulation Board Block Diagram

The **DNMEG_V6HXT** is a complete network interface solution featuring high speed serial IOs. The **DNMEG_V6HXT** can be used stand-alone, without hosting (contact factory for chassis options if required) hosted by 8-lane PCIe cable (GEN1/GEN2) plugged into ASIC Prototyping boards from the DINI product line as an expansion peripheral. FPGA configuration and other miscellaneous board functions are controlled by the NXP LPC1754 ARM based microcontroller, including the front panel LCD.

A single **DNMEG_V6HXT** configured with the Xilinx Virtex-6, XC6VHXT565T FPGA, can emulate up to 4 million gates of logic as measured by a reasonable ASIC gate counting standard. This gate count estimate number does not include embedded memories and multipliers resident in each FPGA. One hundred percent (100%) of the FPGA resources are available to the user application, but the user's application must include all necessary MACs and the PCIe Bridge. The **DNMEG_V6HXT** achieves high gate density and allows for fast target clock frequencies by utilizing FPGAs from Xilinx's 40nm Virtex-6 HXT family.

### Virtex-6 HXT FPGAs from Xilinx

The **DNMEG_V6HXT** is configured with a Xilinx Virtex-6, HXT family FPGA, in the FFG1923 package. This package supports 720 IOs and all are utilized. The HXT FPGAs contain high-speed transceiver PHYs of two different types. GTX transceivers

are capable of handling data rates of 150 MB/s to 6.5 Gb/s, making these useful for lower speed Ethernet, Serial ATA, and GEN1/GEN2 PCI Express. The GTH transceivers are tuned higher, 2.48 to 11.18 Gb/s, making them applicable to 10 gigabit Ethernet (10 GbE). Two possible FPGAs can be stuffed: XC6VHX380T or the XC6VHX565T. The XC6VHX380T comes in three speeds grades, with -3 being the fastest. The larger XC6VHX565T is limited to the -2 speed grade. This means the smaller device can be clocked at a higher frequency at the cost of slightly fewer FPGA logic resources. The XC6VHX565T is capable of handling >4M ASIC gates of logic and is among the largest of the FPGAs shipping from any vendor in 2011. Features of the Virtex-6 HXT FPGAs include the efficient, dual-register 6-input look-up table (LUT) logic, 18 Kb (2 x 9 Kb) block RAMs and second generation DSP48E1 slices (includes 25 x 18 multipliers). Floating point functions can be implemented using these DSP slices.

### Network Prototyping with FPGAs at the High End

#### 40GbE/100GbE with CFP Module

The **DNMEG_V6HXT** hosts a single **C Form-factor pluggable** (CFP) module that is connected to 10-lanes of GTH transceivers. A variety of CFP MSA fiber optic transceiver modules (not supplied) are compatible to this connector and provide PHYS for 40Gb/s and 100Gb/s applications. The user is required to provide the MAC IP for the FPGA.

#### 40GbE with QSFP+

The **DNMEG_V6HXT** has two **Quad Small Form Factor Pluggable** (QSFP+) connectors. Each QSFP+ is attached to 4-lanes of GTH transceivers. A variety of QSFP+ PHYS can be used here, creating a single lane of 40GbE, or 4-lanes of 10GbE. The user is required to provide the MAC IP for the FPGA.

#### 10GbE with SFP+

The **DNMEG_V6HXT** has four **Small Form Factor Pluggable** (SFP+) connectors, each attached to single GTH lane. Again, a variety of SFP+ PHYS can be used here, with the most popular being 10GbE.

**10/100/1000 BaseT with SFP** Eight SFP connectors are attached to single GTX lane. A variety of SFP PHYS can be used here, with the most popular being 1000BaseT.

#### Two Serial-ATA Ports (SATA II)

The FPGA has dual SATA II (Serial ATA II) connectors attached to GTX. With SATA IP integrated into the FPGA logic, SATA cables connected can provide additional high-speed data paths to off board peripheral.

#### GTX Expansion Header

Eight lanes of GTX are connected to our standard GTX expansion header (purple thing in block diagram). Daughter cards such as the DNSEAM_SFP can be used here to add

8 SFP sockets, potentially adding 1x/2x/4x Fibre Channel, 10/100/1000GbE Ethernet, XAUI, SATA or Serial RapidI/O to the mix.

All or any subset of the above interfaces high speed serial interfaces can be used simultaneously. Two GTH channels are connected to high-speed SMAs.

**DDR3 - Bulk Memory**
A single PC3-8500 DDR3 UDIMM socket enables up to 16GB (plus ECC) of memory for bulk storage and lookup. With a 16GB UDIMM memory stick, the configuration is 2048M x 72. Using a -2 or -3 speed grade FPGA, this interface is tested at the maximum FPGA IO frequency: 533 MHz (1066 Mb/s with DDR). You are welcome to use this memory as 64-bits with 8 bits of error correction (ECC), or as a 72-bit memory without correction.

This is the same UDIMM interface used in our blockbuster DNPCIe_10G_HXT_LL product. To minimize data synchronization across clock boundaries, important for networking applications, it probably makes sense to clock this DDR3 interface at a 3x multiple of the base Ethernet frequency of 156.25 MHz, which is 468.75 MHz. A 3x phase synchronous clock can be easily generated internal to the FPGA, allowing zero latency synchronous data transfers between the Ethernet packet receiving logic and the DDR3 memory controller. The DDR3 controller can be optimized in any way you choose. Dini Group provide several Verilog examples, at no charge. All functions of the DDR3 DRAM can be exploited and optimized. Up to 8 banks can be open at once. Timing variables such as CAS latency and precharge can be tailored to the minimum given your operating frequency and the timing specification of the exact DDR3 memory utilized.

Alternate UDIMM memories are in development, including an RLDRAM and a QDRII+ option.

**Daughter cards for customization and expansion: MEG-Array and FMC**

**MEG-Array**
Two 400-pin FCI MEG-Array connectors are attached to a single interface on the FPGA. One MEG-Array connector is on the top and one the bottom. The signals are shared. The bottom connector is used when this card is designated as a peripheral to our ASIC prototyping product. The top connector is used when this card is used stand-alone and application of one of our many DNMEG daughter cards is useful. This is a non-proprietary, industry standard connector and the mating connector is readily available. Dini Group can provide the mating connector at cost custom User daughter cards. The 192 signals (96 pairs) to/from each of these MEG-Array expansion connectors are routed differentially and can run at the limit of the Virtex-6 FPGA IOs: 710 MHz. Clocks, resets, and presence detection, along with abundant (fused) power are included in each connector.

**FMC (Vita-57)**
FPGA Mezzanine Card, or FMC, as defined in VITA 57, provides a specification describing an IO mezzanine module with connection to an FPGA or other device with reconfigurable IO capability. Most vendors of FMC daughter cards tend to ignore the specification, making this interface standard a questionable option. Also, the total number of IOs in the specification is much too small. But there are some good A/D and D/A cards that adhere enough to the specification to be useful.

**Easy Configuration via PCIe, USB, or Ethernet**
Configuration of the FPGAs is under the control of an embedded CPU, an ARM-based LPC1754 from NXP. Xilinx is not nice enough to supply a serial PROM large enough to configure the XC6VHXT565T, so we need to use rather exotic methods to create enough onboard EEPROM storage for this function.

**Status LEDs, Debug**
As with all of our ASIC emulation boards, the **DNMEG_V6HXT** is loaded with LEDs. The LEDs are stuffed in several different colors (red, green, blue, orange et al.). Blinking these LEDs in a controlled fashion can confuse a trout. While this is unlikely to be fatal to the little fish, make sure an adult is present and wear eye protection when testing this feature. These LEDs are user controllable from the FPGAs so can be used as visual feedback in addition to the task of distracting fish. A JTAG connector provides an interface to ChipScope, Veridae, and other third party debug tools.

# 1 FPGA (Virtex-6)

## 1.1 Overview

Virtex-6 FPGAs are the programmable silicon foundation for Targeted Design Platforms that deliver integrated software and hardware components to enable designers to focus on innovation as soon as their development cycle begins. Using the third-generation ASMBL (Advanced Silicon Modular Block) column based architecture, the Virtex-6 family contains multiple distinct sub-families. This overview covers the devices in the LXT, SXT, and HXT sub-families. Each sub-family contains a different ratio of features to most efficiently address the needs of a wide variety of advanced logic designs. In addition to the high-performance logic fabric, Virtex-6 FPGAs contain many built-in system-level blocks. These features allow logic designers to build the highest levels of performance and functionality into their FPGA-based systems. Built on a 40 nm state-of-the art copper process technology, Virtex-6 FPGAs are a programmable alternative to custom ASIC technology. Virtex-6 FPGAs offer the best solution for addressing the needs of high-performance logic designers, high-performance DSP designers, and high-performance embedded systems designers with unprecedented logic, DSP, connectivity, and soft microprocessor capabilities. For more information, please reference the Xilinx Virtex-6 documentation.

## 1.2 Summary of Virtex-6 FPGA Features

- Three sub-families:
  - Virtex-6 LXT FPGAs: High-performance logic with advanced serial connectivity
  - Virtex-6 SXT FPGAs: Highest signal processing capability with advanced serial connectivity
  - Virtex-6 HXT FPGAs: Highest bandwidth serial connectivity
- Compatibility across sub-families
  - LXT and SXT devices are footprint compatible in the same package
- Advanced, high-performance FPGA Logic
  - Real 6-input look-up table (LUT) technology
  - Dual LUT5 (5-input LUT) option
  - LUT/dual flip-flop pair for applications requiring rich register mix
  - Improved routing efficiency
  - 64-bit (or 32 x 2-bit) distributed LUT RAM option
  - SRL32/dual SRL16 with registered outputs option
- Powerful mixed-mode clock managers (MMCM)
  - MMCM blocks provide zero-delay buffering, frequency synthesis, clock-phase shifting, input-jitter filtering, and phase-matched clock division
- 36-Kb block RAM/FIFOs
  - Dual-port RAM blocks
  - Programmable
  - Dual-port widths up to 36 bits
  - Simple dual-port widths up to 72 bits
  - Enhanced programmable FIFO logic
  - Built-in optional error-correction circuitry
  - Optionally use each block as two independent 18 Kb blocks
- High-performance parallel SelectIO technology
  - 1.2 to 2.5V I/O operation

  - Source-synchronous interfacing using
  - ChipSync™ technology
  - Digitally controlled impedance (DCI) active termination
  - Flexible fine-grained I/O banking
  - High-speed memory interface support with integrated write-leveling capability
- Advanced DSP48E1 slices
  - 25 x 18, two's complement multiplier/accumulator
  - Optional pipelining
  - New optional pre-adder to assist filtering applications
  - Optional bitwise logic functionality
  - Dedicated cascade connections
- Flexible configuration options
  - SPI and Parallel Flash interface
  - Multi-bitstream support with dedicated fallback reconfiguration logic
  - Automatic bus width detection
- System Monitor capability on all devices
  - On-chip/off-chip thermal and supply voltage monitoring
  - JTAG access to all monitored quantities
- Integrated interface blocks for PCI Express® designs
  - Designed to the PCI Express Base Specification 2.0
  - Gen1 (2.5 Gb/s) and Gen2 (5 Gb/s) support with GTX transceivers
  - Endpoint and Root Port capable
  - x1, x2, x4, or x8 lane support per block
- GTX transceivers: 150 Mb/s to 6.6 Gb/s
- GTH transceivers: 2.488 Gb/s to beyond 11 Gb/s
- Integrated 10/100/1000 Mb/s Ethernet MAC block
  - Supports 1000BASE-X PCS/PMA and SGMII using GTX transceivers
  - Supports MII, GMII, and RGMII using SelectIO technology resources

- 2500Mb/s support available

- 40 nm copper CMOS process technology
- 1.0V core voltage (-1, -2, -3 speed grades only)
- Lower-power 0.9V core voltage option (-1L speed grade only)
- High signal-integrity flip-chip packaging available in standard or Pb-free package options

## 1.3 FPGA Configuration (Virtex-6)

Virtex-6 FPGAs are configured by loading application-specific configuration data - the bitstream - into internal memory. Because the Xilinx FPGA configuration memory is volatile, it must be configured each time it is powered-up. The bitstream is loaded into the device through special configuration pins. These configuration pins serve as the interface for a number of different configuration modes. The following configuration modes are supported:

- Slave SelectMAP (parallel) configuration mode (x8)
- JTAG/Boundary-Scan configuration mode

The configuration modes are explained in detail in Chapter 2, Configuration Interfaces of the UG360 - Virtex-6 FPGA Configuration User Guide. The specific configuration mode is selected by setting the appropriate level on the dedicated Mode input pins M[2:0]. The M2, M1, and M0 mode pins should be set at a constant DC voltage level, either through pull-up or pull-down resistors, or tied directly to ground or VCC_CONFIG, see Figure 4. The mode pins should not be toggled during and after configuration. The mode pins can also be driven by the Microcontroller (MCU) in Slave SelectMAP mode. The mode pins should not be toggled during and after configuration.

In Slave SelectMAP mode, the FPGA is configured via the Microcontroller (MCU). The mode pins can also be driven by the MCU, see Figure 4.

### 1.3.1 Mode Select Resistors M[2..0]

The specific configuration mode is selected by setting the appropriate level on the dedicated Mode input pins M[2:0] configuration pins.

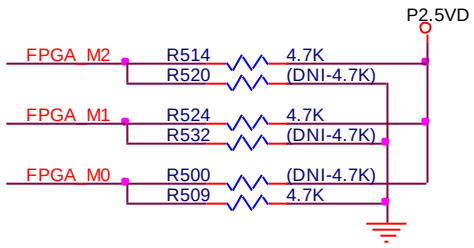



Figure 4 – Mode Select Resistors M[2..0] (default Slave SelectMAP)

Select the configuration scheme by driving the FPGA M[2..0] pins either HIGH or LOW as shown in Table 3.

Table 3 – FPGA Configuration Schemes

| Configuration Mode | M[2:0] | Configuration Resistors |
|---|---|---|
| Slave SelectMAP | 110 | R514, R524, R509 Installed |
| JTAG | 101 | R514, R532, R500 Installed |

### 1.3.2 In-System Programming using a Microcontroller (MCU)

The NXP, LPC1754 Microcontroller (U26) is connected to the SelectMAP interface on FPGA (U34) with a dedicated 8-bit bidirectional data bus. This allows for faster data transfer during configuration or readback. CCLK is an input in Slave SelectMAP mode and is sourced from the MCU. Table 4 shows the SelectMAP bus connection between the Microcontroller and the FPGA.

Table 4 – SelectMAP Bus between Microcontroller and FPGA

| Signal Name | MCU | FPGA |
|---|---|---|
| FPGA_D0 | U26-51 | U34-BB35 |
| FPGA_D1 | U26-52 | U34-BA35 |
| FPGA_D2 | U26-53 | U34-AM35 |
| FPGA_D3 | U26-54 | U34-AL34 |
| FPGA_D4 | U26-55 | U34-AV34 |
| FPGA_D5 | U26-58 | U34-AU34 |
| FPGA_D6 | U26-59 | U34-AK33 |
| FPGA_D7 | U26-60 | U34-AJ33 |
| FPGA_CCLK | U26-73 | U34-AC33 |
| FPGA_PROGN | U26-76 | U34-U33 |
| FPGA_BUSY | U26-70 | U34-AE33 |
| FPGA_RD/WRN | U26-74 | U34-W33 |
| FPGA_INITN | U26-72 | U34-T14 |
| FPGA_CSN | U26-75 | U34-AA33 |
| FPGA_DONE | U26-71 | U34-T13 |
| FPGA_M0 | U26-36 | U34-V32 |
| FPGA_M1 | U26-35 | U34-T32 |
| FPGA_M2 | U26-32 | U34-T33 |

### 1.3.3 JTAG

Virtex-6 devices support IEEE standards 1149.1 and 1532. IEEE 1532 is a standard for In-System Configuration (ISC), based on the IEEE 1149.1 standard. JTAG is an acronym for the Joint Test Action Group, the technical subcommittee initially responsible for developing the standard. This standard provides a means to ensure the board-level integrity of individual components and the interconnections between them. The IEEE 1149.1 Test Access Port and Boundary-Scan Architecture is commonly referred to as JTAG. JTAG connector (J30) is used to download the configuration files to the FPGA, see Figure 5.

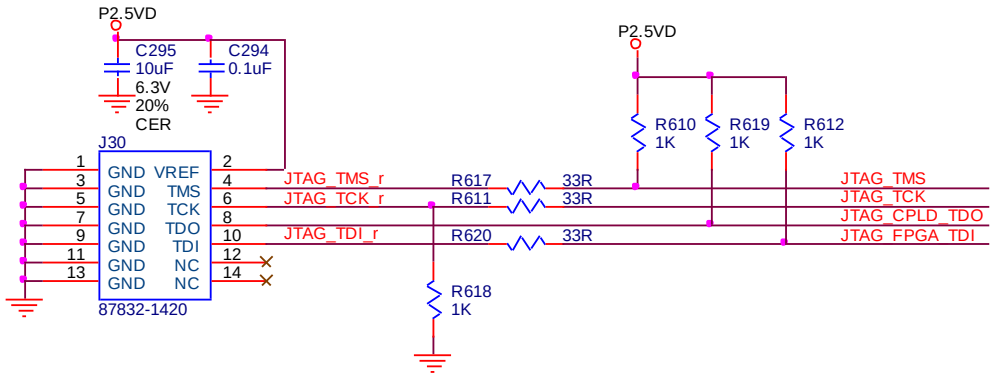



Figure 5 – FPGA JTAG Interface

Table 5 shows the connection between the JTAG header and the FPGA.

Table 5 – Connection between JTAG Header and the FPGA

| Signal Name | Header | FPGA |
|---|---|---|
| JTAG_FPGA_TCK | J30-6 -> U51-9 | U34-AB12 |
| JTAG_FPGA_TDI | J30-10 | U34-AF12 |
| JTAG_FPGA_TDO | J30-8 | U34-Y12 |
| JTAG_FPGA_TMS | J30-4 -> U51-18 | U34-AD12 |

Note: The TMS and TCK signals are buffered before being distributed to the CPLD and FPGA.

## 1.4 DDR3 Memory (UDIMM)

A 240 pin UDIMM module, connected to the Virtex-6 FPGA, allows addressing for up to 16GB DDR3 SDRAM (PC3-8500) modules. The following transfer speed can be expected:

- Speed Grade -3 1066Mb/s
- Speed Grade -2 1066Mb/s

- Speed Grade -1 800Mb/s

The UDIMM interface is connected to IO Banks on the Virtex-6 FPGAs and uses a 1.5V switching power supply for $V_{DD}$ and $V_{CCIO}$. $V_{TT}$ and $V_{REF}$ are powered from a separate linear power supply set at 0.75V. DDR3 SDRAM modules are available from Micron, example part number for a 8GB (1Gb x 72) 240-pin UDIMM SDRAM module is: MT18KSF1G72AZ-1G4D1.

### 1.4.1 DDR3 SDRAM Memory Interface Solution

The Virtex-6 FPGA memory interface solutions core is a pre-engineered controller and physical layer (PHY) for interfacing Virtex-6 FPGA user designs to DDR2 and DDR3 SDRAM devices. Figure 6 shows a high-level block diagram of the Virtex-6 FPGA memory interface solution connecting a user design to a DDR2 or DDR3 SDRAM device. The physical layer (PHY) side of the design is connected to the DDR2 or DDR3 SDRAM device via FPGA I/O blocks (IOBs), and the user interface (UI) side is connected to the user design via FPGA logic. Alternatively, an AXI4 slave interface is available to connect to an AXI4 master (not shown in Figure 6).

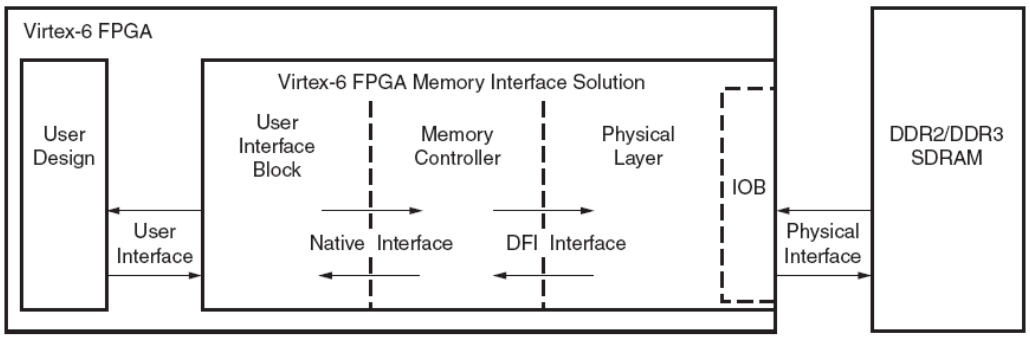


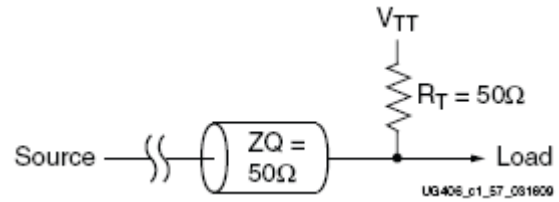

Figure 6 - DDR2/DD3 SDRAM Memory Interface Solution

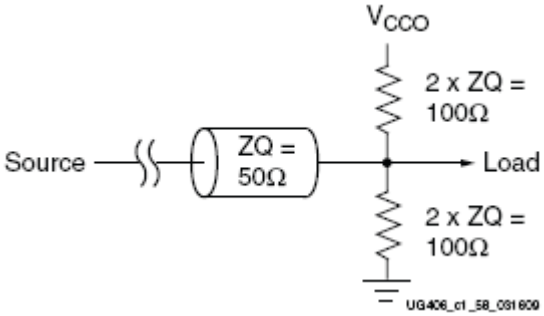
The Memory Interface Generator (MIG) is a self-explanatory wizard tool that can be invoked under the CORE Generator software. Xilinx published a memory application note; please refer to *UG-406 - Virtex-6 FPGA Memory Interface Solutions, User Guide*.

### 1.4.2 Design Guidelines - DDR3 Termination

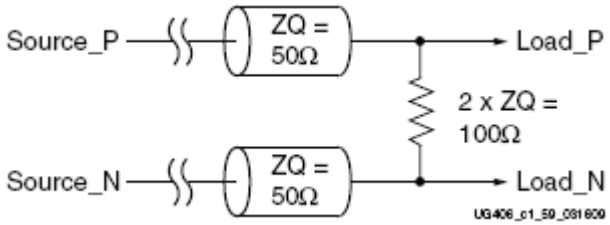
These rules apply to termination for DDR3 SDRAM:

- Unidirectional signals are to be terminated with the memory device's internal termination or a pull-up of 50Ω to VTT at the load. A split 100Ω termination to VCCO and a 100Ω termination to GND can be used, but takes more power. For bidirectional signals, the termination is needed at both ends of the signal (DCI/ODT or external termination).




- Differential signals should be terminated with the memory device's internal termination or a 100Ω differential termination at the load. For bidirectional signals, termination is needed at both ends of the signal (DCI/ODT or external termination).




- All termination must be placed as close to the load as possible. The termination can be placed before or after the load provided that the termination is placed within a small distance of the load pin. The allowable distance can be determined by simulation.
- DCI can be used at the FPGA as long as the DCI rules such as VRN/VRP are followed.
- The RESET and CKE signals are not terminated. These signals should be pulled down during memory initialization with a 4.7 kΩ resistor connected to GND.
- ODT, which terminates a signal at the memory, and DCI, which terminates a signal at the FPGA, are required. The MIG tool should be used to specify the configuration of the memory system for setting the mode register properly. Refer to Micron technical note TN-47-01 for additional details on ODT.
- ODT applies to the DQ, DQS, and DM signals only. If ODT is used, the mode register must be set appropriately to enable ODT at the memory.

### 1.4.3 Design Guidelines – DDR3 IO Standards

These rules apply to the I/O standard selection for DDR3 SDRAMs:

- Designs generated by the MIG tool use the SSTL15_T_DCI and DIFF_SSTL15_T_DCI standards for all bidirectional I/O (DQ, DQS).

- The SSTL15 and DIFF_SSTL15 standards are used for unidirectional outputs, such as control/address, and forward memory clocks.

The MIG tool creates the UCF using the appropriate standard based on input from the GUI.

### 1.4.4 UDIMM Switching Power Supply (+1.5V)

The Texas Instruments PTH08T230WAZ POLA DC-DC Converter is used to create the $V_{DD}$ supply for the DDR3 UDIMM, set to +1.5V @ 6A, see Figure 7.

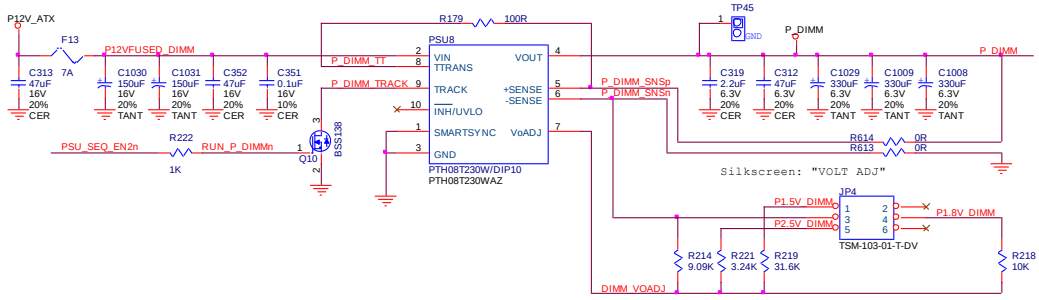



Figure 7 – UDIMM Switching Power Supply (+1.5V)

### 1.4.5 VTT Linear Power Supply (+0.75V)

The Texas Instruments TPS51200 is a sink/source double data rate (DDR) termination regulator for termination of DDR3 UDIMMs, see Figure 8.

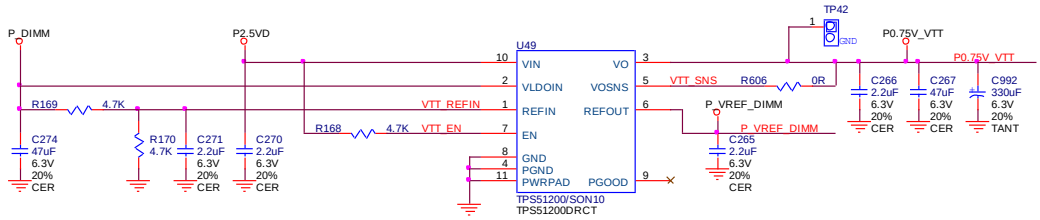



Figure 8 - VTT Linear Power Supply (+0.75V)

### 1.4.6 Serial Presence-Detect EEPROM Operation

DDR3 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to comply with JEDEC Standard JC-45, "Appendix X: Serial Presence-Detect (SPD) for DDR3 SDRAM Modules." These bytes identify module-specific timing parameters, configuration information, and physical attributes. User-specific information can be

written into the remaining 128 bytes of storage. READ/WRITE operations between the system (master) and the EEPROM (slave) device occur via a standard I2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA[2:0], which provide four unique DIMM/EEPROM addresses. Write protect (WP) is connected to Vss internal to the Temp Sensor/EEPROM, permanently disabling hardware write protection. Please note that VDDSPD is connected to +3.3V.

Table 6 - Serial Presence-Detect EEPROM Connections

| Signal Name | FPGA | DDR3 UDIMM |
|---|---|---|
| DIMM_SA0 | NC | J29-117, pull-down R604 |
| DIMM_SA1 | U34-G17 | J29-237, pull-down R605 |
| DIMM_SA2 | NC | J29-119, pull-down R175 |
| DIMM_SCL | U34-AT35 | J29-118, pull-up R174 |
| DIMM_SDA | U34-AU35 | J29-238, pull-up R172 |

### 1.4.7 Clocking Connections between FPGA and UDIMM

The clocking connections between the FPGA and the UDIMM connector are shown in Table 7.

Table 7 – Clocking Connections between FPGA and the UDIMM Connector

| Signal Name | FPGA | UDIMM |
|---|---|---|
| DIMM_CK0P | U34-N22 | J29-184 |
| DIMM_CK0N | U34-N21 | J29-185 |
| DIMM_CK1P | U34-M24 | J29-63 |
| DIMM_CK1N | U34-M25 | J29-64 |

### 1.4.8 Connections between FPGA and UDIMM

Table 8 shows the connections between the FPGA and the UDIMM connector pins.

Table 8 - Connections between FPGA and the UDIMM Connector

| Signal Name | FPGA | UDIMM |
|---|---|---|
| DIMM_A0 | U34-B19 | J29-188 |
| DIMM_A1 | U34-L22 | J29-181 |
| DIMM_A10 | U34-A20 | J29-70 |
| DIMM_A11 | U34-C26 | J29-55 |
| DIMM_A12 | U34-B20 | J29-174 |
| DIMM_A13 | U34-M19 | J29-196 |

| Signal Name | FPGA | UDIMM |
|---|---|---|
| DIMM_A14 | U34-E22 | J29-172 |
| DIMM_A15 | U34-B24 | J29-171 |
| DIMM_A2 | U34-D21 | J29-61 |
| DIMM_A3 | U34-M22 | J29-180 |
| DIMM_A4 | U34-J21 | J29-59 |
| DIMM_A5 | U34-K22 | J29-58 |
| DIMM_A6 | U34-C21 | J29-178 |
| DIMM_A7 | U34-B26 | J29-56 |
| DIMM_A8 | U34-C22 | J29-177 |
| DIMM_A9 | U34-D26 | J29-175 |
| DIMM_BA0 | U34-H19 | J29-71 |
| DIMM_BA1 | U34-L20 | J29-190 |
| DIMM_BA2 | U34-L23 | J29-52 |
| DIMM_CASN | U34-E18 | J29-74 |
| DIMM_CB0 | U34-G24 | J29-39 |
| DIMM_CB1 | U34-F25 | J29-40 |
| DIMM_CB2 | U34-P23 | J29-45 |
| DIMM_CB3 | U34-P24 | J29-46 |
| DIMM_CB4 | U34-J24 | J29-158 |
| DIMM_CB5 | U34-H24 | J29-159 |
| DIMM_CB6 | U34-N23 | J29-164 |
| DIMM_CB7 | U34-N24 | J29-165 |
| DIMM_CK0N | U34-N21 | J29-185 |
| DIMM_CK0P | U34-N22 | J29-184 |
| DIMM_CK1N | U34-M25 | J29-64 |
| DIMM_CK1P | U34-M24 | J29-63 |
| DIMM_CKE0 | U34-C23 | J29-50 |
| DIMM_CKE1 | U34-D25 | J29-169 |
| DIMM_DM0 | U34-G27 | J29-125 |
| DIMM_DM1 | U34-D29 | J29-134 |
| DIMM_DM2 | U34-F29 | J29-143 |
| DIMM_DM3 | U34-D23 | J29-152 |

| Signal Name | FPGA | UDIMM |
|---|---|---|
| DIMM_DM4 | U34-A19 | J29-203 |
| DIMM_DM5 | U34-D20 | J29-212 |
| DIMM_DM6 | U34-J18 | J29-221 |
| DIMM_DM7 | U34-K17 | J29-230 |
| DIMM_DM8 | U34-G25 | J29-161 |
| DIMM_DQ0 | U34-C29 | J29-3 |
| DIMM_DQ1 | U34-B29 | J29-4 |
| DIMM_DQ10 | U34-H28 | J29-18 |
| DIMM_DQ11 | U34-H29 | J29-19 |
| DIMM_DQ12 | U34-F27 | J29-131 |
| DIMM_DQ13 | U34-P28 | J29-132 |
| DIMM_DQ14 | U34-K26 | J29-137 |
| DIMM_DQ15 | U34-K27 | J29-138 |
| DIMM_DQ16 | U34-T27 | J29-21 |
| DIMM_DQ17 | U34-R27 | J29-22 |
| DIMM_DQ18 | U34-J28 | J29-27 |
| DIMM_DQ19 | U34-J29 | J29-28 |
| DIMM_DQ2 | U34-N27 | J29-9 |
| DIMM_DQ20 | U34-L27 | J29-140 |
| DIMM_DQ21 | U34-N28 | J29-141 |
| DIMM_DQ22 | U34-L28 | J29-146 |
| DIMM_DQ23 | U34-L29 | J29-147 |
| DIMM_DQ24 | U34-L24 | J29-30 |
| DIMM_DQ25 | U34-L25 | J29-31 |
| DIMM_DQ26 | U34-E23 | J29-36 |
| DIMM_DQ27 | U34-D24 | J29-37 |
| DIMM_DQ28 | U34-B25 | J29-149 |
| DIMM_DQ29 | U34-A25 | J29-150 |
| DIMM_DQ3 | U34-M27 | J29-10 |
| DIMM_DQ30 | U34-J23 | J29-155 |
| DIMM_DQ31 | U34-H23 | J29-156 |
| DIMM_DQ32 | U34-M21 | J29-81 |

| Signal Name | FPGA | UDIMM |
|---|---|---|
| DIMM_DQ33 | U34-M20 | J29-82 |
| DIMM_DQ34 | U34-R20 | J29-87 |
| DIMM_DQ35 | U34-P20 | J29-88 |
| DIMM_DQ36 | U34-B22 | J29-200 |
| DIMM_DQ37 | U34-A22 | J29-201 |
| DIMM_DQ38 | U34-G22 | J29-206 |
| DIMM_DQ39 | U34-F22 | J29-207 |
| DIMM_DQ4 | U34-C27 | J29-122 |
| DIMM_DQ40 | U34-R23 | J29-90 |
| DIMM_DQ41 | U34-R22 | J29-91 |
| DIMM_DQ42 | U34-R21 | J29-96 |
| DIMM_DQ43 | U34-P21 | J29-97 |
| DIMM_DQ44 | U34-F20 | J29-209 |
| DIMM_DQ45 | U34-E20 | J29-210 |
| DIMM_DQ46 | U34-K21 | J29-215 |
| DIMM_DQ47 | U34-J20 | J29-216 |
| DIMM_DQ48 | U34-C18 | J29-99 |
| DIMM_DQ49 | U34-C17 | J29-100 |
| DIMM_DQ5 | U34-C28 | J29-123 |
| DIMM_DQ50 | U34-H17 | J29-105 |
| DIMM_DQ51 | U34-G16 | J29-106 |
| DIMM_DQ52 | U34-P19 | J29-218 |
| DIMM_DQ53 | U34-N19 | J29-219 |
| DIMM_DQ54 | U34-F19 | J29-224 |
| DIMM_DQ55 | U34-F18 | J29-225 |
| DIMM_DQ56 | U34-J16 | J29-108 |
| DIMM_DQ57 | U34-K18 | J29-109 |
| DIMM_DQ58 | U34-M17 | J29-114 |
| DIMM_DQ59 | U34-L17 | J29-115 |
| DIMM_DQ6 | U34-N26 | J29-128 |
| DIMM_DQ60 | U34-N16 | J29-227 |
| DIMM_DQ61 | U34-M16 | J29-228 |

| Signal Name | FPGA | UDIMM |
|---|---|---|
| DIMM_DQ62 | U34-R16 | J29-233 |
| DIMM_DQ63 | U34-P16 | J29-234 |
| DIMM_DQ7 | U34-M26 | J29-129 |
| DIMM_DQ8 | U34-F28 | J29-12 |
| DIMM_DQ9 | U34-E28 | J29-13 |
| DIMM_DQS0N | U34-A27 | J29-6 |
| DIMM_DQS0P | U34-B27 | J29-7 |
| DIMM_DQS1N | U34-P25 | J29-15 |
| DIMM_DQS1P | U34-R25 | J29-16 |
| DIMM_DQS2N | U34-A29 | J29-24 |
| DIMM_DQS2P | U34-A28 | J29-25 |
| DIMM_DQS3N | U34-F24 | J29-33 |
| DIMM_DQS3P | U34-F23 | J29-34 |
| DIMM_DQS4N | U34-G21 | J29-84 |
| DIMM_DQS4P | U34-H22 | J29-85 |
| DIMM_DQS5N | U34-G20 | J29-93 |
| DIMM_DQS5P | U34-H21 | J29-94 |
| DIMM_DQS6N | U34-P18 | J29-102 |
| DIMM_DQS6P | U34-R18 | J29-103 |
| DIMM_DQS7N | U34-R17 | J29-111 |
| DIMM_DQS7P | U34-T17 | J29-112 |
| DIMM_DQS8N | U34-H26 | J29-42 |
| DIMM_DQS8P | U34-J26 | J29-43 |
| DIMM_EVENTN | U34-F17 | J29-187 |
| DIMM_NC | NC | J29-135, J29-126 |
| DIMM_NC0 | U34-R26 | J29-144, J29-48 |
| DIMM_NC1 | U34-P26 | J29-153, J29-49 |
| DIMM_NC2 | U34-A24 | J29-162, J29-53 |
| DIMM_NC3 | NC | J29-68, R608-2 |
| DIMM_NC4 | NC | J29-79, R609-2 |
| DIMM_ODT0 | U34-D18 | J29-195 |
| DIMM_ODT1 | U34-K16 | J29-77 |

| Signal Name | FPGA | UDIMM |
|---|---|---|
| DIMM_RASN | U34-G19 | J29-192 |

### 1.4.9 UDIMM Trace Lengths

The UDIMM traces are length matched, and routed to the following lengths refer to Table 9:

Table 9 – UDIMM PCB Trace Lengths

| Signal Name | Routed Length (mm) | Description |
|---|---|---|
| DIMM_CK0N | 128.14 | Clock group |
| DIMM_A0 | 128.38 | Control group |
| DIMM_DQ0 | 128.18 | Data byte group |

## 1.5 EEPROM

The AT24C256C (U23) provides 262,144-bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 32,768 words of eight bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential.

### 1.5.1 EEPROM Circuit Diagram

Figure 9 shows the implementation of the EEPROM memory circuit.

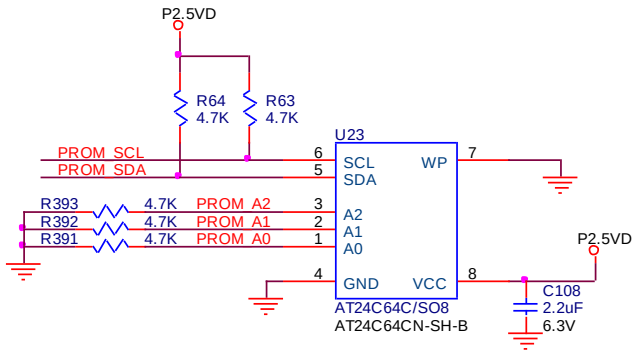



Figure 9 –FPGA EEPROM

Device address (A2, A1, and A0) is set up by discrete resistors and is mapped to 1010000x, where "x" is the R/W bit The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is HIGH, and a write operation is initiated if this bit is LOW.

### 1.5.2 Connections between FPGA and the EEPROM

The connections between the FPGA and the EEPROM are shown in Table 10.

Table 10 - Connections between FPGA and the EEPROM

| Signal Name | FPGA | EEPROM |
|---|---|---|
| PROM_SCL | U34-AP35 | U23-6 |
| PROM_SDA | U34-AR35 | U23-5 |
| PROM_A0 | | R391 |
| PROM_A1 | | R392 |
| PROM_A2 | | R393 |

## 1.6 RS232 Port

A RS232 serial port (U29) is provided for low speed communication with the Virtex-6 FPGA and the MCU. The LTC2804 is a dual RS-232 transceiver in narrow SSOP and chip-scale DFN package. An integrated DC-to-DC converter generates power supplies for driving RS-232 levels. A logic supply pin allows easy interfacing with different logic levels independent of the DC-DC supply. Part is compatible with the TIA/EIA-232-F standard.

### 1.6.1 RS232 Circuit Diagram

Figure 10 shows the implementation of the serial port.

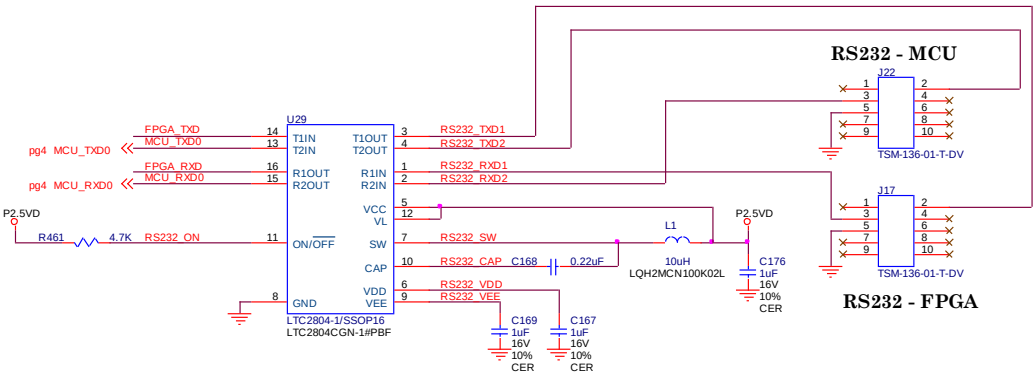



Figure 10 –FPGA/MCU Serial Port

The two signals that are relevant to the FPGA are:

- Transmit Data - FPGA_TXD
- Receive Data - FPGA_RXD

### 1.6.2 Connections between FPGA and the RS232 Port

The connections between the FPGA and the RS232 Port are shown in Table 11.

Table 11 - Connections between RS232 Port and the FPGA

| Signal Name | FPGA | RS232 |
|---|---|---|
| FPGA_TXD | U34-BC33 | U29-14 |
| FPGA_RXD | U34-BD33 | U29-16 |

## 1.7 Backup Battery

The encryption key memory cells are volatile and must receive continuous power to retain their contents. During normal operation, these memory cells are powered by the auxiliary voltage input (VCCAUX), although a separate VBATT power input is provided for retaining the key when VCCAUX is removed. Because VBATT draws very little current (on the order of nanoamperes), a small watch battery is suitable for this supply. (To estimate the battery life, refer to *DS152 - Virtex-6 FPGA Data Sheet - DC and Switching Characteristics*. At less than a 150 nA load, the endurance of the battery should be limited only by its shelf life. VBATT does not draw any current and can be removed while VCCAUX is applied. VBATT cannot be used for any purpose other than retaining the encryption keys when VCCAUX is removed. Backup Batteries are available Panasonic, Lithium Coin Cell, 3V 40mAH from Digi-Key, P/N CR1220.

### 1.7.1 Backup Battery Circuit

The recommended battery voltage is specified at +1.0V to +2.5V. The TPS782 low-dropout regulator (LDOs) offers the benefits of ultra-low power ($I_Q$ = 1µA), see Figure 11.

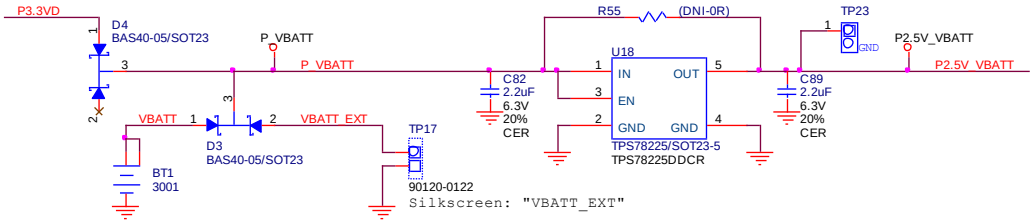



Figure 11 - Backup Battery Supply

### 1.7.2 Backup Battery Loads

The backup battery supplies the following loads, see Table 12.

Table 12 – Backup Battery Load

| Signal Name | Load | Description |
|---|---|---|
| P2.5V_VBATT | U34-AA13 | FPGA encryption supply. |

## 1.8 VCCINT Switching Power Supply

A distributed point of load (POL) power supply topology is implemented utilizing the PTH08T250W is a high-performance 50-A rated, non-isolated power module operating

from an input voltage range of 4.5 V to 14 V. The PTH08T250W requires a single resistor (R671) to set the output voltage to +1.0V, see Figure 12.

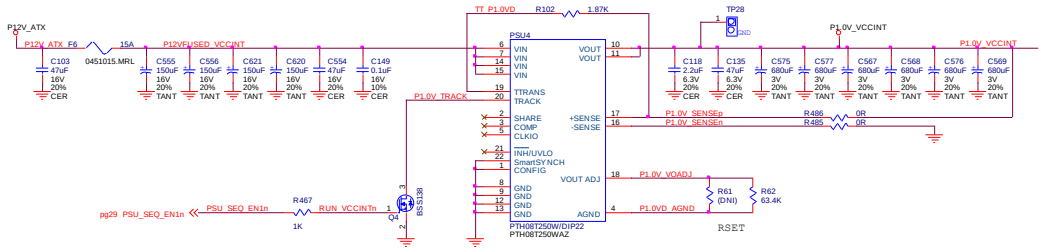



Figure 12 – VCCINT Switching Supply for the FPGA

Note: Heat sinking on the FPGA was designed for worst-case conditions. Both and active and passive solution are provided for when the board is rack mounted.

# 2 MCU

The NXP, LPC1754 is provided to configure the FPGA via SelectMAP from a USB Flash drive and other miscellaneous housekeeping functions, including the LCD Display. The LPC1754 is an ARM Cortex-M3 based microcontroller for embedded applications featuring a high level of integration and low power consumption. The LPC1754 operate at frequencies of up to 100 MHz. The MCU code and functionality is not available to the user, and only the relevant subsections will be addressed.

## 2.1 USB Interface

The LPC1754 includes a USB 2.0 full-speed device/Host/OTG controller with dedicated DMA controller and on-chip PHY for device, Host, and OTG functions. The USB port (J42) is configured as a Host, used for configuration with a USB Flash Drive. The USB signals are routed as differential traces and connect to the LPC1754 via a common mode filter (T1), see Table 13.

Table 13 – USB Interconnect

| Signal Name | MCU | USB |
|---|---|---|
| USB_D_p | U26-22 | J42-3 |
| USB_D_n | U26-23 | J42-2 |

The NUP2201MR6 (D7) transient voltage suppressor is designed to protect the high speed data lines from ESD. The AP2161 (U56) is an integrated high-side power switch optimized for Universal Serial Bus (USB) and other hot-swap applications.

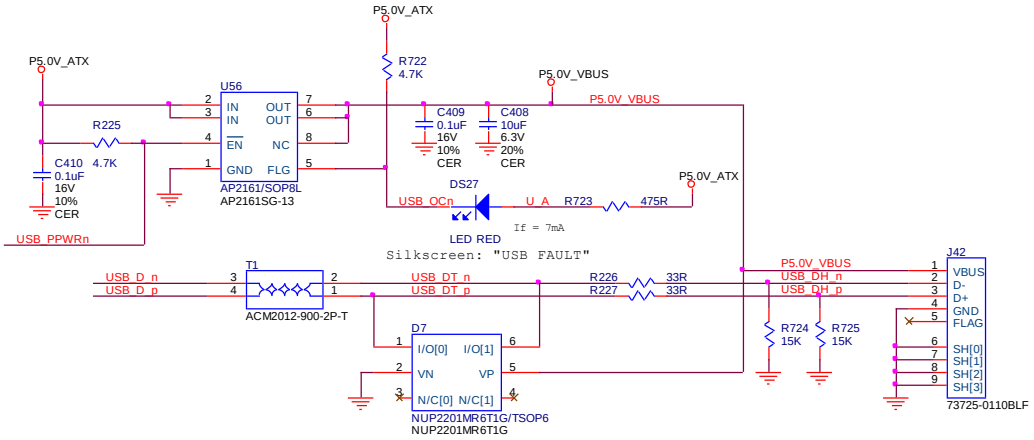



Figure 13 - USB2.0 Host (Type A)

The AP2161 offer current (1.5A) and thermal limiting and short circuit protection as well as controlled rise time and under-voltage lockout functionality.

## 2.2 LCD – Serial Port (RS232)

A dedicated RS232 serial port (U52) is provided for low speed communication with the Matrix Orbital LCD Display P/N GLK19264-7T-1U-FGW. The LTC2804 is a dual RS-232 transceiver in narrow SSOP and chip-scale DFN package. An integrated DC-to-DC converter generates power supplies for driving RS-232 levels. A logic supply pin allows easy interfacing with different logic levels independent of the DC-DC supply. Part is compatible with the TIA/EIA-232-F standard.

### 2.2.1 RS232 Circuit Diagram

Figure 10 shows the implementation of the serial port.

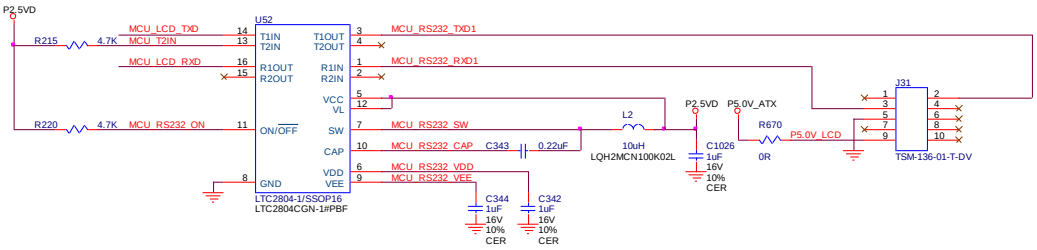



Figure 14 –LCD – Serial Port (RS232)

The two signals that are relevant to the LCD are:

- Transmit Data - MCU_LCD_TXD
- Receive Data - MCU_LCD_RXD

### 2.2.2 Connections between MCU/LCD and the RS232 Port

The connections between the MCU/LCD and the RS232 Port are shown in Table 11.

Table 14 - Connections between MCU/LCD and the RS232 Port

| Signal Name | MCU/LCD | RS232 |
|---|---|---|
| MCU_LCD_TXD | U26-39 | U52-14 |
| MCU_LCD_RXD | U26-40 | U52-16 |
| MCU_RS232_TXD1 | J31-2 | U52-3 |
| MCU_RS232_RXD1 | J31-3 | U52-1 |

## 2.3 Temperature Monitor

The MCU monitors the FPGA temperature using the MAX6639 (U42). The MAX6639 monitors its own temperature and the FPGA diode-connected transistor. The 2-wire serial interface accepts standard System Management Bus (SMBus™) write byte, read byte, send byte, and receive byte commands to read the temperature data and program the alarm thresholds. Temperature data can be read at any time over the SMBus, and three programmable alarm outputs can be used to generate interrupts, throttle signals, or over-temperature shutdown signals.

The temperature data is also used by the internal dual PWM fan-speed controller to adjust the speed of up to two cooling fans (J1/J26), thereby minimizing noise when the system is running cool, but providing maximum cooling when power dissipation increases. Speed control is accomplished by tachometer feedback from the fan, so that the speed of the fan is controlled, not just the PWM duty cycle. Accuracy of speed measurement is 4%.

The maximum recommended operating temperature of the FPGA is 85 degrees. When the MCU measures the temperature above 80 degrees, it will immediately RESET and clear the FPGA.

### 2.3.1 Temperature Sensor Circuit

Each FPGA is connected to the temperature sensor (U24). This sensor measures the temperature of the FPGA silicon die, see Figure 15. The maximum recommended operating temperature of the FPGA is 85 degrees (commercial rating). When the configuration circuitry measures the temperature of any FPGA above 80 degrees, it will immediately un-configure the FPGA, and prevent it from re-configuring.

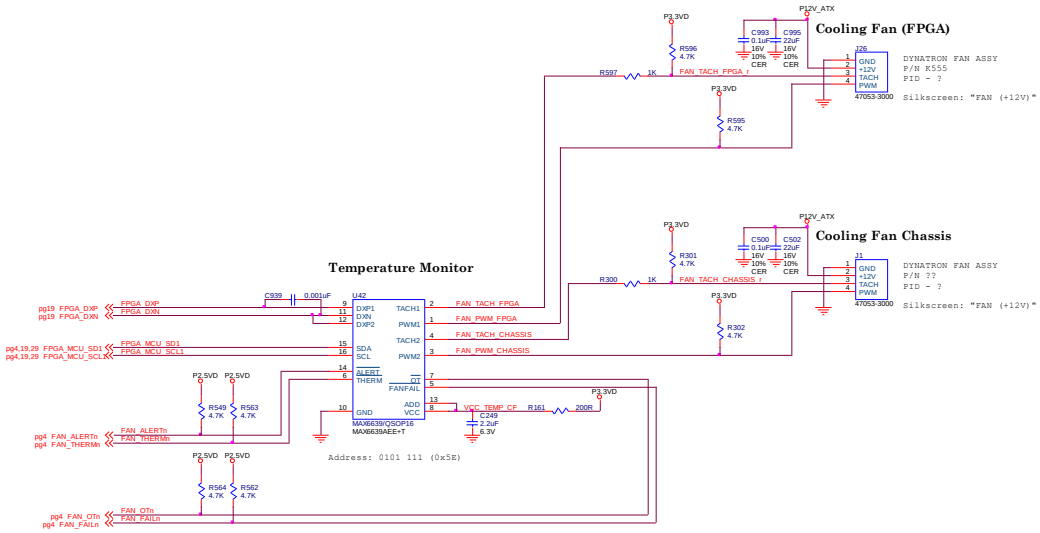



Figure 15 – FPGA Temperature Sensor

### 2.3.2 Connection between the MCU and the Temperature Sensor

The connection between the MCU (U26) and the Temperature Sensor (U42) are shown in Table 15. Note that the temperature sensor can be read by the MCU (U26), FPGA (U34) or the Platform Manager (U33).

Table 15 - Connection between MCU and the Temperature Sensor

| Signal Name | Temp Sensor | MCU/FPGA/PM |
|---|---|---|
| FPGA_MCU_SD1 | U42-15 | U26-37 / U34-AH32 / U33-M2 |
| FPGA_MCU_SCL1 | U42-16 | U26-38 / U34-AH33 / U33-N2 |

## 2.4 Emulation and Debugging

Standard JTAG test/debug interface as well as Serial Wire Debug and Serial Wire Trace Port options are provided. Debug and trace functions are integrated into the ARM Cortex-M3. Serial wire debug and trace functions are supported in addition to a standard JTAG debug and parallel trace functions. The ARM Cortex-M3 is configured to support up to eight breakpoints and four watch points. Figure 16 shows J16, the JTAG connector used to debug the NXP, LPC1754.

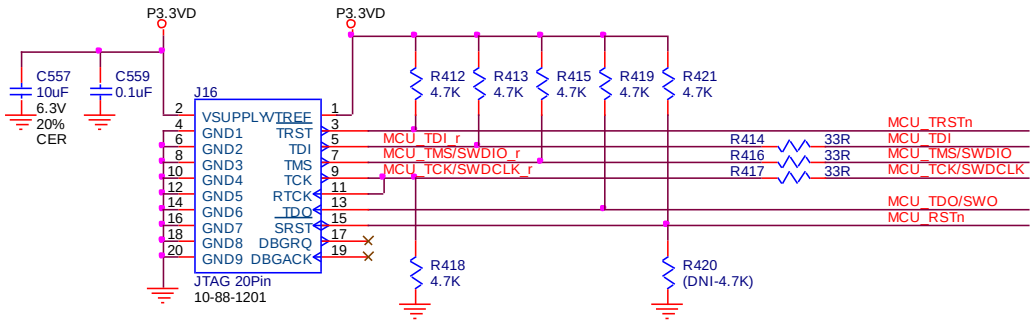



Figure 16 – MCU Trace/Debug Header

Table 16 shows the connection between the MCU JTAG connector and the NXP, LPC1754.

Table 16 – JTAC connection to the LPC1754

| Signal Name | JTAG Connector | MCU |
|---|---|---|
| MCU_TCK/SWDCLK | J16-9 | U26-M5 |
| MCU_TDI | J16-5 | U26-2 |
| MCU_TDO/SWO | J16-13 | U26-1 |
| MCU_TMS/SWDIO | J16-7 | U26-3 |
| MCU_RSTn | J16-15 | U26-14 |
| MCU_TRSTn | J16-3 | U26-4 |

# 3 Clocking Networks

## 3.1 Clock Methodology

The DNMEG_V6HXT has a flexible and configurable clocking scheme. Figure 17 is a block diagram showing the clocking resources and connections. All of the clock networks on the DNMEG_V6HXT are routed point-to-point using dedicated differential (LVPECL) traces. Since LVPECL is a low voltage-swing differential signal, using a single ended input buffer in the FPGA will not work. An example Verilog implementation of a differential clock input is given below:

```
IBUFDS  #(.DIFF_TERM("TRUE"))
    clk_sys_ibufgds_inst (.I(CLK_SYS_BUF2P), .IB(CLK_SYS_BUF2N),
        .O(clk_sys_ibufgds));
```

The pin assignment in the UCF file:

```
NET "CLK_SYS_BUF2P" loc =AN33;
NET "CLK_SYS_BUF2N" loc =AP34;
```

Due to limited resources, no clock test points are provided to the user.

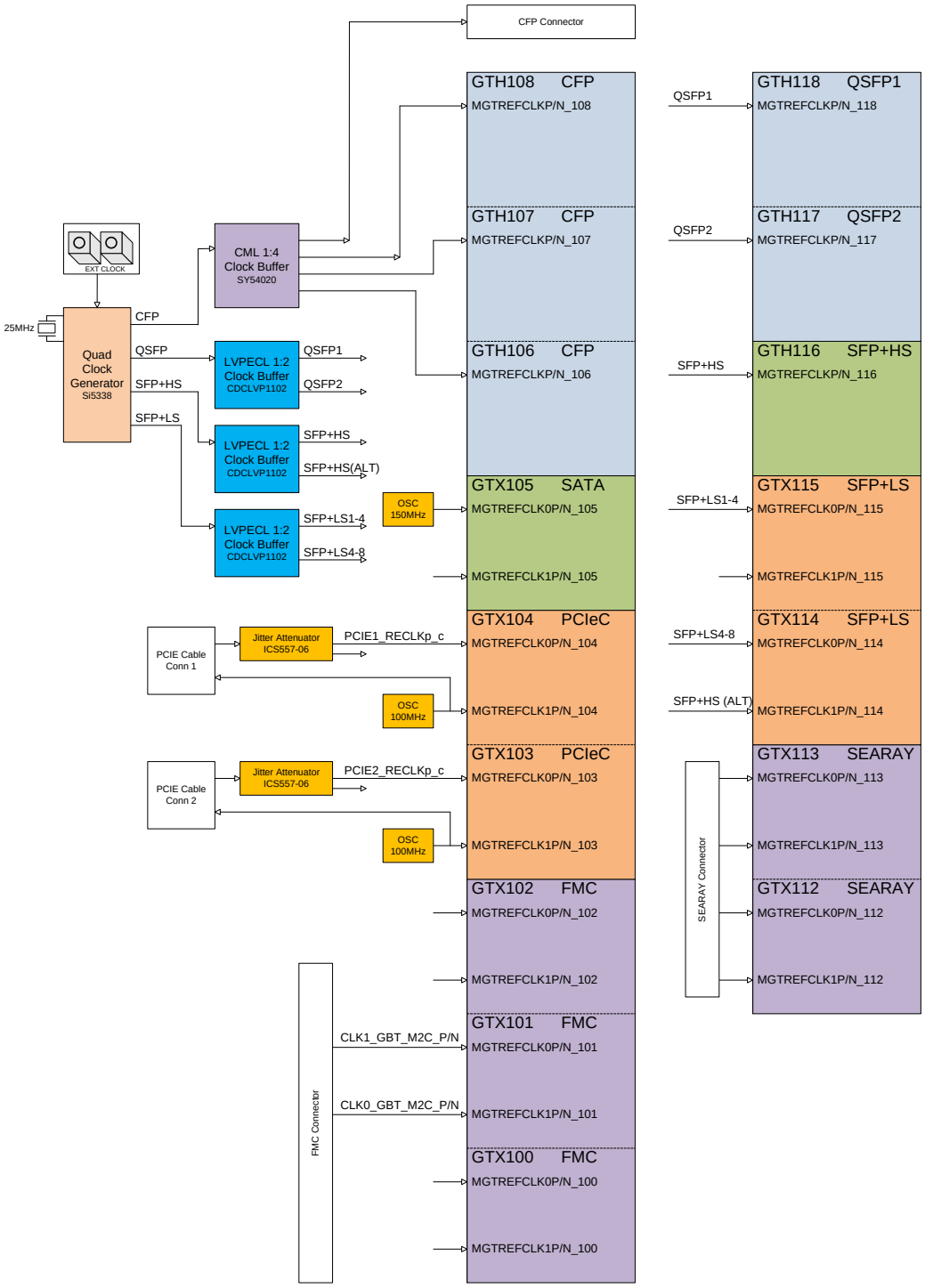



Figure 17 - Clocking Block Diagram

- GTX/GTH Transceiver Clocks
  - CFP

  - QSFP
  - SFP+ HS (High Speed)
  - SFP+ LS (Low Speed)
- PCI Express Cable Clock (100MHz)
  - System Clock
  - PCI Express Channel 1/2
- SATA II Oscillator (150MHz)
- External Clock (LVDS) Input via SMA (x2)
- Daughter Card Header Clocks (MEG-Array)
  - DCA_CLK_DN_IN_P/N_TOP
  - DCA_CLK_UP_OUT_P/N_TOP
  - DCA_CLK_DN_IN_P/N_BOT
  - DCA_CLK_UP_OUT_P/N_BOT
- FMC Mezzanine Card Clocks
  - CLK0_GBT_M2C_P/N
  - CLK1_GBT_M2C_P/N

## 3.2 GTX/GTH Transceiver Clocks

The Si5338 is a high-performance, low-jitter clock generator capable of synthesizing any frequency on each of the device's four output drivers. This timing IC is capable of replacing up to four different frequency crystal oscillators or operating as a frequency translator. Using its patented MultiSynth technology, the Si5338 allows generation of four independent clocks with 0 ppm precision.

Each output clock is independently configurable to support various signal formats and supply voltages. The Si5338 provides low-jitter frequency synthesis in a space-saving 4 x 4 mm QFN package. The device is programmable via an I2C/SMBus-compatible serial interface and supports operation from a 1.8, 2.5, or 3.3 V core supply. I2C device programming is made easy with the ClockBuilder Desktop software available at www.silabs.com/ClockBuilder.

### 3.2.1 GTX/GTH Transceiver Clock Circuit

Each one of the four clock outputs from the Si5338 (U47) is connected to a LVPECL buffer, that in-turn provides clock sources to the GTX/GTH Transceivers:

- CFP
- QSFP

- SFP+ HS (High Speed)
- SFP+ LS (Low Speed)

Figure 18 shows the clock generator circuit. LED (DS14) is used to indicate PLL Loss of Lock (PLL_LOL).

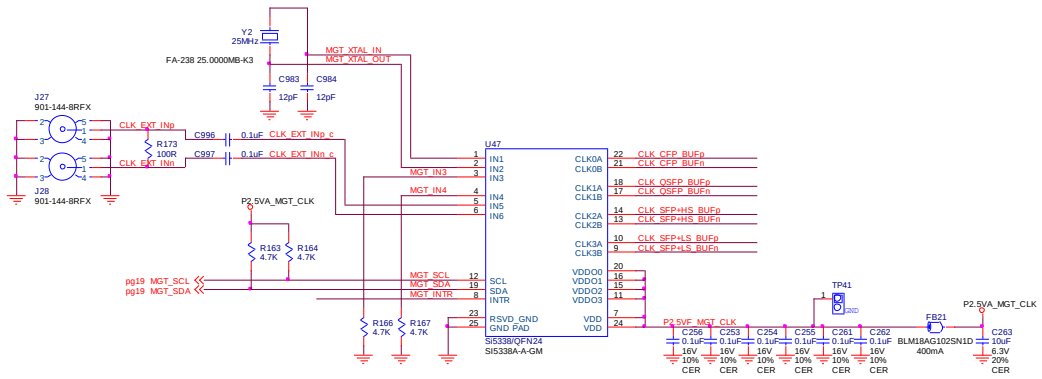



Figure 18 – GTX/GTH Clock Circuit

### 3.2.2 Input Connections to the Clock Generator

Input connections to the Clock Generator are shown in Table 17. The GTX/GTH Clock Generator, Si5338, provides support for an external clock input via IN5/IN6 pins. The SMA (J27, J28) inputs are AC-coupled and terminated for a 100Ω differential input.

Table 17 - Input connections to the Clock Generator

| Signal Name | Input | Clock Generator |
|---|---|---|
| **SMA** | | |
| CLK_EXT_INp | J27 | U47-5 |
| CLK_EXT_INn | J28 | U47-6 |
| **I2C** | | |
| MGT_SCL | U34-AT33 | U47-12 |
| MGT_SDA | U34-AT34 | U47-19 |

### 3.2.3 Output Connections between the Clock Buffers and the FPGA

All of the clock networks on the DNMEG_V6HXT are routed point-to-point using dedicated differential (LVPECL) traces. The arrival times of the clock edges at each FPGA are phase-aligned (length-matched on the PCB) within about 100ps. These clocks are all suitable for synchronous communication. The connections between the FPGA and the Clock Buffers are shown in Table 18.

Table 18 - Connections between the Clock Buffers and the FPGA

| Signal Name | Clock Buffer | FPGA |
|---|---|---|
| **CFP Clocks (CML)** | | |
| CLK_CFP_REFCLKP | U41-15 | J25-146 |
| CLK_CFP_REFCLKN | U41-14 | J25-147 |
| CLK_CFP_MGT106P | U41-7 | U34-R41 |
| CLK_CFP_MGT106N | U41-6 | U34-R42 |
| CLK_CFP_MGT107P | U41-10 | U34-J41 |
| CLK_CFP_MGT107N | U41-9 | U34-J42 |
| CLK_CFP_MGT108P | U41-12 | U34-E41 |
| CLK_CFP_MGT108N | U41-11 | U34-E42 |
| **QSFP Clocks (LVPECL)** | | |
| CLK_QSFP_MGT117P | U40-11 | U34-J4 |
| CLK_QSFP_MGT117N | U40-12 | U34-J3 |
| CLK_QSFP_MGT118P | U40-9 | U34-E4 |
| CLK_QSFP_MGT118N | U40-10 | U34-E3 |
| **SFP+ HS (High Speed) Clocks (LVPECL)** | | |
| CLK_SFP+HS_MGT116P | U37-9 | U34-R4 |
| CLK_SFP+HS_MGT116N | U37-10 | U34-R3 |
| CLK_SFP+HS_MGT114P_ALT | U37-11 | U34-Y10 |
| CLK_SFP+HS_MGT114N_ALT | U37-12 | U34-Y9 |
| **SFP+ LS (Low Speed) Clocks (LVPECL)** | | |
| CLK_SFP+LS_MGT114P | U32-9 | U34-AB10 |
| CLK_SFP+LS_MGT114N | U32-10 | U34-AB9 |
| CLK_SFP+LS_MGT115P | U32-11 | U34-V10 |
| CLK_SFP+LS_MGT115N | U32-12 | U34-V9 |

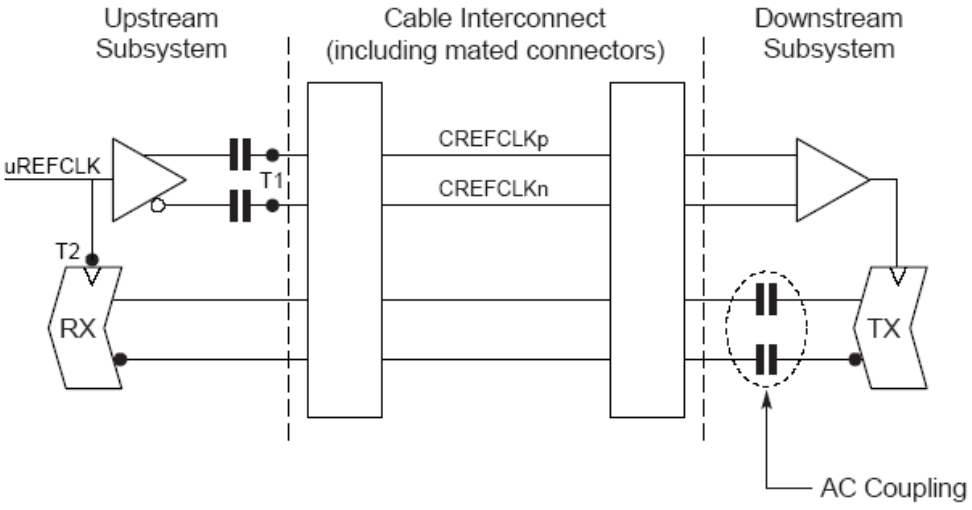
Note: The maximum, clock frequency for the Si5338 clock generator is 710MHz. Only two unique frequencies above 350 MHz can be simultaneously output, Fvco/4 and Fvco/6. See "3.3. Synthesis Stages" on page 17 of the datasheet.

## 3.3 PCI Express Cable Reference Clocks (HCSL)

To control jitter, radiated emissions, and crosstalk, and allow for future silicon fabrication process changes, a low voltage swing, current mode, differential clock is specified. Isolated power domains, between the two Subsystems, are maintained through

implementation of AC-coupling capacitors at the source. Supplying the cable reference clock is required from an Upstream Subsystem.

- Upstream Device, Clock from local PCI Express Clock Buffer (U14)
- Downstream Device, Clock from remote REFCLK on cable, Buffered (U16)




A dedicated oscillator (X1) - 100MHz, is buffered to provide all the possible clocking requirements, see Figure 19.

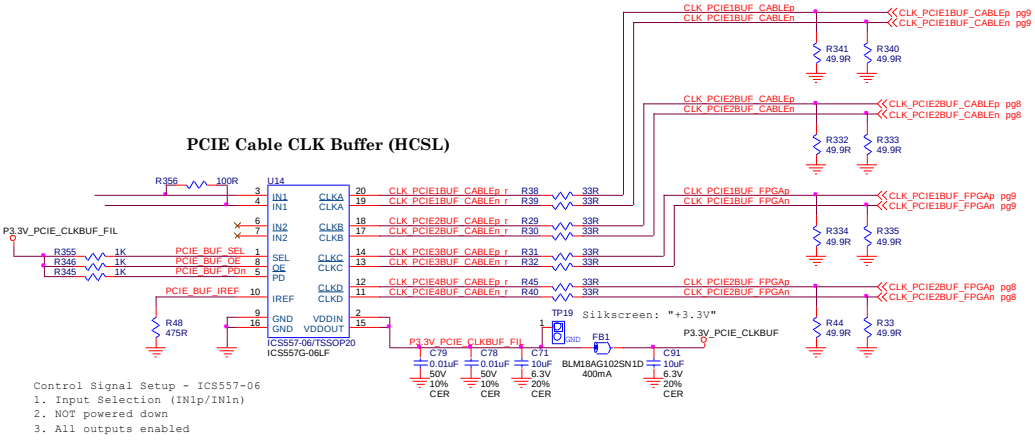



Figure 19 – PCI Express Cable Reference Clock Buffer (HCSL)

## PCI Express Clock Jitter Attenuator (Upstream to Downstream)

In addition, a resistor/capacitor network is provided for the user to select the source/destination of the clock signals, see Figure 20.

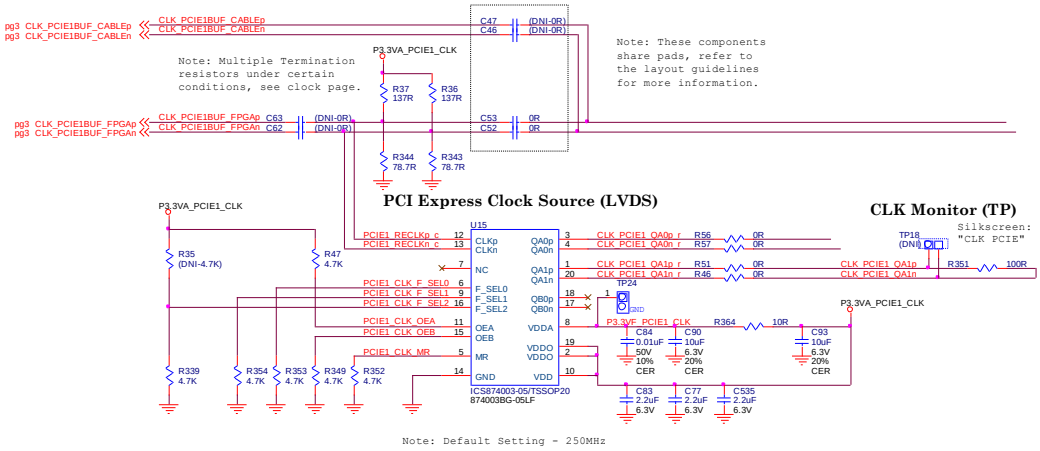

PCI Express Clock Source (LVDS)
CLK Monitor (TP)
Note: Multiple Termination resistors under certain conditions, see clock page.
Note: These components share pads, refer to the layout guidelines for more information.
Note: Default Setting - 250MHz

Figure 20 – PCI Express Clock Jitter Attenuator

### 3.3.1 Selecting between Upstream or Downstream (Auxiliary Signals)

In order to toggle between upstream and downstream mode, DIP switches on the board need to be set.

- To set PCIE Cable Connection, Port 0-3, to Upstream Mode - turn ON all switches on dipswitch (S1). Turn OFF dipswitch S3-1.
- To set PCIE Cable Connection, Port 0-3, to Downstream mode - turn OFF all switches on dipswitch (S1). Turn ON dipswitch S3-1.
- To set PCIE Cable Connection, Port 4-7, to Upstream Mode - turn ON all switches on dipswitch (S2). Turn OFF dipswitch S3-2.
- To set PCIE Cable Connection, Port 4-7, to Downstream mode - turn OFF all switches on dipswitch (S2). Turn ON dipswitch S3-2.

Note: PCIEx_FPGA_CPRSNT /PCIEx_FPGA_CPWRON is an active LOW signal in "To Slave Upstream)" mode and an active HIGH signal when in "From Host (Downstream) mode. It is also possible to permanently enable CPRSNT (cable present) detection when running in downstream mode by stuffing R330 (Port 0-3) or R329 (Port 4-7) with a 0Ω resistor.

### 3.3.2 Connection between the PCI Express Jitter Attenuator and the FPGA

The connection between the PCI Express Jitter Attenuator (U15/U16) and the GTX Transceiver on the FPGA are shown in Table 19. These signals are routed as differential pairs (LVDS) and are AC-coupled.

Table 19 - Connection between the PCI Express Jitter Attenuator and the FPGA

| Signal Name | Jitter Attenuator | FPGA |
|---|---|---|

| | Connector | |
|---|---|---|
| CLK_OSC_PCIE1_GTPp | U15-3 | U34-AB35 |
| CLK_OSC_PCIE1_GTPn | U15-4 | U43-AB36 |
| CLK_OSC_PCIE2_GTPp | U16-3 | U34-AF35 |
| CLK_OSC_PCIE2_GTPn | U16-4 | U43-AF36 |

## 3.4 SATA II Clock Oscillator (LVDS)

A dedicated LVDS oscillator is provided for the SATA II interface. The oscillator is powered from a +2.5V LDO, and provides a reference clock to the GTX Transceiver on the FPGA, see Figure 21. The oscillator power supply (U28) is filtered to reduce power supply noise and jitter. The SATA II Clock Oscillator is assigned as follows:

- SATA II (X2) – 150MHz P/N LV7745DW-150.0M

The Pletronics LV77D Series 2.5V Clock Oscillators are recommended for this application and is available in frequencies from 1MHz to 325MHz from Nu Horizons.

### 3.4.1 SATA II Clock Oscillator

The differential oscillator (X2) outputs are AC-coupled to the GTX Transceiver on the FPGA, see Figure 21.

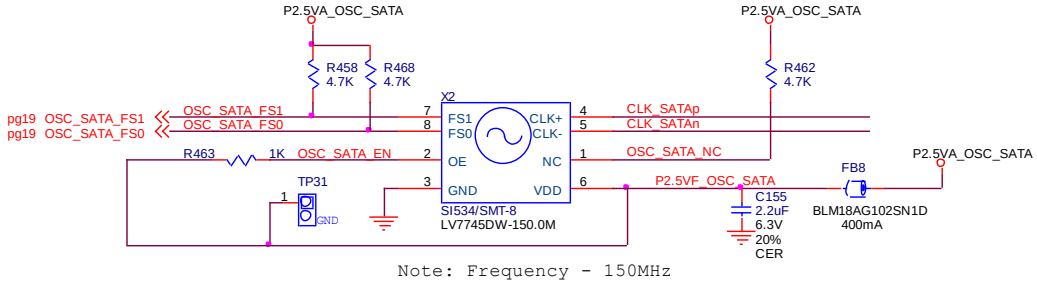



Figure 21 – SATA II Clock Oscillator

### 3.4.2 Connection between SATA II Clock Oscillator and the FPGA

The connections between the SATA II Clock Oscillator and the FPGA are shown in Table 20. These signals are routed as differential pairs (LVDS) and are AC-coupled.

Table 20 - Connection between SATA II Clock Oscillator and the FPGA

| Signal Name | SATA II OSC | FPGA |
|---|---|---|
| CLK_SATAp | X2-4 | U34-V35 |
| CLK_SATAn | X2-5 | U34-V36 |

## 3.5 Daughter Card Header Clocks (MEG-Array)

The 400-pin MEG-Array connector (P2) on the bottom of the PCB is used to interface to Dini Group Daughter Cards, e.g. DNMEG_Obs, this allows for IO expansion. The IO signals are shared, with the exception of the clocks. The daughter card header provides a dedicated LVDS clock input (from daughter card) connected to "clock capable" pins on the FPGA and a dedicated LVDS clock output (input to daughter card). In addition, each IO bank provides a source synchronous LVDS clock that connects to the FPGA. The 400 pin MEG-Array connector (P1) on the bottom of the PCBA is used to interface to Dini Group products, e.g. DN2076K10.

### 3.5.1 Daughter Card Global Clock Input/Output

DCA_CLK_DN_INp/n_TOP is a global LVDS input clock to the FPGA (IO Bank 24) and DCA_CLK_UP_OUTp/n_TOP is a global LVDS output clock from the FPGA (IO Bank 24), see Figure 22. Note: These signals are routed as differential pairs (LVDS) and are NOT AC-coupled. Refer to the *Xilinx Virtex-6 Data Sheet* for IO levels and provide DC isolation on the daughter card if required.

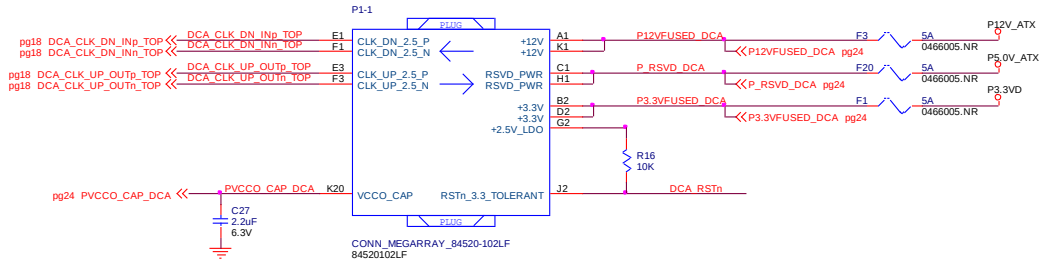



Figure 22 – Daughter Card Global Clock Input/Output

"DCA_CLK_FB_P/N" is looped back from an output of the FPGA to a clock input on the same FPGA (IO Bank 24), see Figure 23.

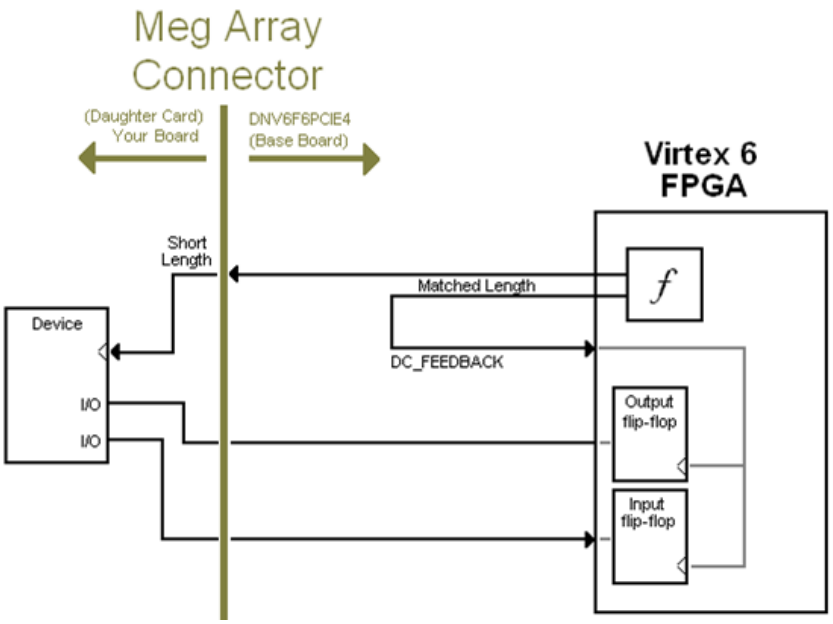



Figure 23 - Daughter Card Header Feedback Clock

The routing length of this feedback clock is equal to the routing length of the signals to the Daughter Card header. This allows the option to have a clock inside the FPGA that is phase aligned with the arrival of the clock at the Daughter Card header.

### 3.5.2 Connection between MEG-Array Daughter Card Clocks and the FPGA

The connection between the Meg-Array Daughter Card clocks and the FPGA are shown in Table 21.

Table 21 - Connections between MEG-Array Daughter Card Clocks and the FPGA

| Signal Name | Daughter Card Header | FPGA |
|---|---|---|
| **TOP Header (P1)** | | |
| DCA_CLK_DN_INP_TOP | U34-J14 | P1-E1 |
| DCA_CLK_DN_INN_TOP | U34-H13 | P1-F1 |
| DCA_CLK_UP_OUTP_TOP | U34-P15 | P1-E3 |
| DCA_CLK_UP_OUTN_TOP | U34-P14 | P1-F3 |
| **BOTTOM Header (P2)** | | |
| DCA_CLK_DN_INP_BOT | U34-AV33 | P2-E1 |
| DCA_CLK_DN_INN_BOT | U34-AW34 | P2-F1 |
| DCA_CLK_UP_OUTP_BOT | U34-AK35 | P2-E3 |
| DCA_CLK_UP_OUTN_BOT | U34-AL35 | P2-F3 |

### 3.5.3 Source Synchronous MEG-Array Daughter Card Clocks

Each Daughter Card IO Bank contains a number of clock capable LVDS pairs. _CC nets connect to SRCC and MRCC pins on the FPGA, while _GCC pins connect to global clock inputs on the FPGA and is capable of clocking all signals on the daughter card using synchronous (zero hold time) timing. Note on Virtex-6, this means a GCC pin, a SRCC or MRCC pin on banks 36, 44, 46, 45 and 47, see Figure 24. These clocks need to comply with the IO requirements of the Virtex-6 FPGA IO bank they are connected too, see schematic for more information.

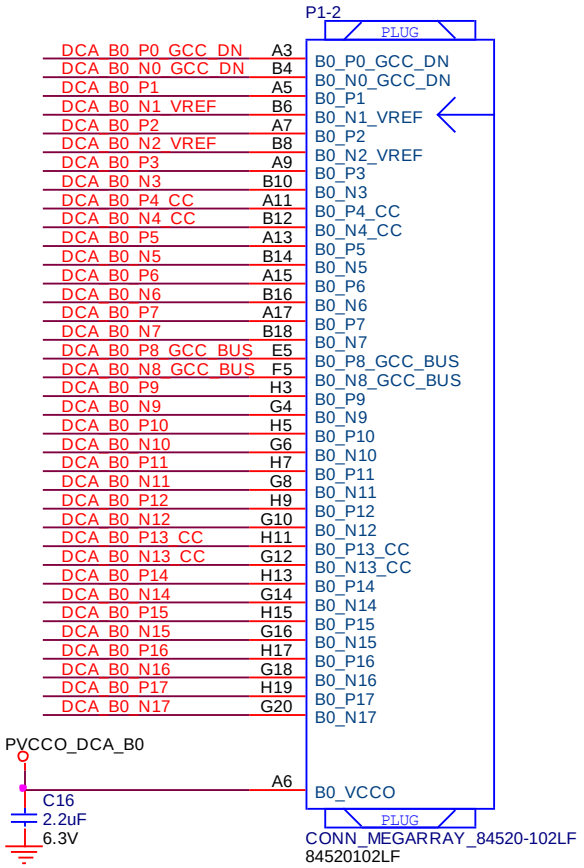



Figure 24 –MEG-Array Daughter Card Clock (Secondary)

### 3.5.4 Connection between MEG-Array Secondary Clocks and the FPGA

The connection between MEG-Array secondary clocks and the FPGA are shown in Table 22. These signals may be used as inter-connect or clocks.

Table 22 - Connections between MEG-Array Secondary Clocks and the FPGA

| Signal Name | DC Headers | FPGA |
|---|---|---|
| **FPGA – Daughter Card Bank 0** | | |

| Signal Name | DC Headers | | FPGA |
|---|---|---|---|
| DCA_B0_P0_GCC_DN | P1-A3 | P2-A3 | U34-BC13 |
| DCA_B0_N0_GCC_DN | P1-B4 | P2-B4 | U34-BC12 |
| DCA_B0_P13_CC | P1-H11 | P2-H11 | U34-AT17 |
| DCA_B0_N13_CC | P1-G12 | P2-G12 | U34-AU16 |
| DCA_B0_P4_CC | P1-A11 | P2-A11 | U34-BB12 |
| DCA_B0_N4_CC | P1-B12 | P2-B12 | U34-BC11 |
| DCA_B0_P8_GCC_BUS | P1-E5 | P2-E5 | U34-BB16 |
| DCA_B0_N8_GCC_BUS | P1-F5 | P2-F5 | U34-BB15 |
| **FPGA – Daughter Card Bank 1** | | | |
| DCA_B1_N10_VREF | P1-J6 | P2-J6 | U34-AN17 |
| DCA_B1_N11_VREF | P1-J8 | P2-J8 | U34-AV13 |
| DCA_B1_P13_CC | P1-K11 | P2-K11 | U34-AJ20 |
| DCA_B1_N13_CC | P1-J12 | P2-J12 | U34-AJ19 |
| DCA_B1_P18_CC | P1-C21 | P2-C21 | U34-AR15 |
| DCA_B1_N18_CC | P1-D22 | P2-D22 | U34-AT15 |
| DCA_B1_P4_CC | P1-C11 | P2-C11 | U34-AU15 |
| DCA_B1_N4_CC | P1-D12 | P2-D12 | U34-AV14 |
| **FPGA – Daughter Card Bank 2** | | | |
| DCA_B2_P12_CC | P1-H29 | P2-H29 | U34-AP13 |
| DCA_B2_N12_CC | P1-G30 | P2-G30 | U34-AR12 |
| DCA_B2_P18_CC | P1-H21 | P2-H21 | U34-AV7 |
| DCA_B2_N18_CC | P1-G22 | P2-G22 | U34-AW6 |
| DCA_B2_P3_CC | P1-A29 | P2-A29 | U34-AU11 |
| DCA_B2_N3_CC | P1-B30 | P2-B30 | U34-AU10 |
| DCA_B2_P8_CC | P1-A39 | P2-A39 | U34-AV9 |
| DCA_B2_N8_CC | P1-B40 | P2-B40 | U34-AW8 |
| **FPGA – Daughter Card Bank 3** | | | |
| DCA_B3_P12_CC | P1-K29 | P2-K29 | U34-AR8 |
| DCA_B3_N12_CC | P1-J30 | P2-J30 | U34-AT7 |
| DCA_B3_P17_CC | P1-K39 | P2-K39 | U34-AR7 |
| DCA_B3_N17_CC | P1-J40 | P2-J40 | U34-AR6 |
| DCA_B3_P3_CC | P1-C29 | P2-C29 | U34-AN11 |

| Signal Name | DC Headers | | FPGA |
|---|---|---|---|
| DCA_B3_N3_CC | P1-D30 | P2-D30 | U34-AP10 |
| DCA_B3_P8_CC | P1-C39 | P2-C39 | U34-AU6 |
| DCA_B3_N8_CC | P1-D40 | P2-D40 | U34-AU5 |
| **FPGA – Daughter Card Bank 4** | | | |
| DCA_B4_P18_CC | P1-E37 | P2-E37 | U34-BB5 |
| DCA_B4_N18_CC | P1-F37 | P2-F37 | U34-BB4 |
| DCA_B4_P6_CC | P1-E19 | P2-E19 | U34-BC6 |
| DCA_B4_N6_CC | P1-F19 | P2-F19 | U34-BD6 |
| DCA_B4_P7_CC | P1-E21 | P2-E21 | U34-BC8 |
| DCA_B4_N7_CC | P1-F21 | P2-F21 | U34-BC7 |
| DCA_B4_P8_CC | P1-E23 | P2-E23 | U34-BA5 |
| DCA_B4_N8_CC | P1-F23 | P2-F23 | U34-BA4 |

## 3.6 FMC Mezzanine Card Clocks

The FMC (also known as VITA 57) standard was developed to provide an industry standard mezzanine form factor in support of a flexible, modular IO interface to an FPGA located on a baseboard or carrier card. It allows the physical IO interface to be decoupled from the FPGA design while maintaining a close coupling between a physical IO interface and an FPGA.

The FMC standard specifies Samtec's SEARAY connector set. The VITA 57 SEAM/SEAF Series system provides 400 IOs in a 40 x 10 configuration or 160 IOs in a selectively loaded 40 x 10 configuration, in 8.5mm and 10mm stack heights. The DNMEG_HXT provides a High Pin Count (HPC) FMC connector, populated with the Samtec's SEARAY socket, P/N ASP-134486-01. The mating part is

CLK[0..1]_M2C_P/N – Differential pairs that are assigned for clock signals, which are driven from the IO Mezzanine Module to the carrier card.

CLK[2..3]_BIDIR_P/N – Differential pairs that are assigned for clock signals, which are driven either by the IO Mezzanine Module or the carrier card.

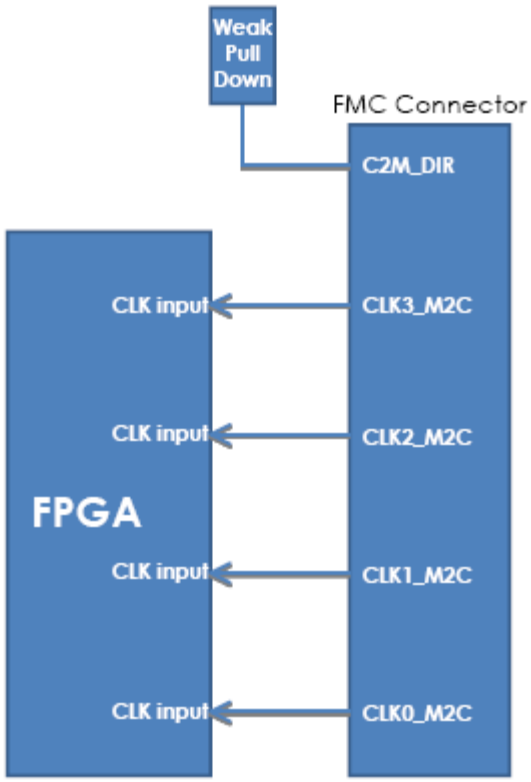
CLK_DIR – Used to determine whether the mezzanine module or the carrier card is the driver for CLK[2..3].

GBTCLK0_M2C_P/N, GBTCLK1_M2C_P/N – A differential pair shall be used as a reference clock for the DP data signals.

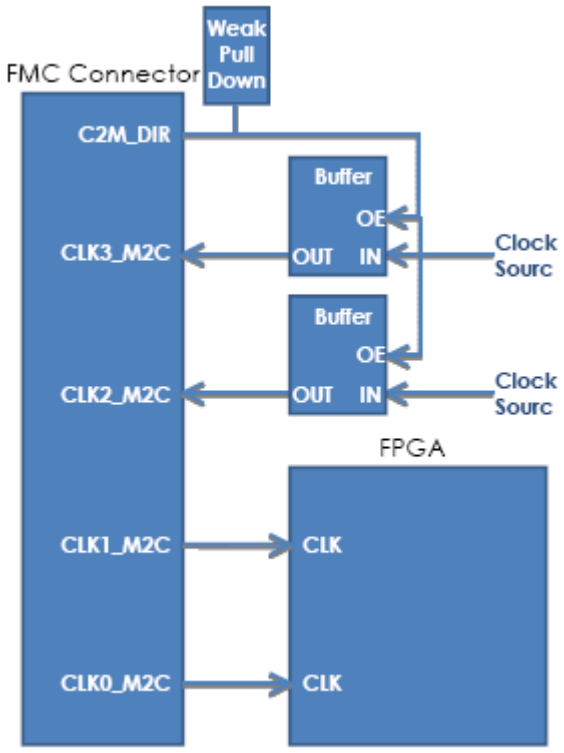
### 3.6.1 FMC Differential Reference Clock Requirements

There are four reference clocks, which have a bus between the carrier card and the IO mezzanine module. The clocks can have two configurations;

1. When 'CLK_DIR' is connected to 'GND.' or unconnected on the mezzanine module, then CLK[0..1]_M2C_P/N, CLK[2..3]_BIDIR_P/N, are four differential pairs that are assigned for clock signals, which are driven from the IO Mezzanine Module to the carrier card (DNMEG_HXT).




2. When 'CLK_DIR' is connected to '3P3V' via a 10K pull up resistor on the mezzanine module, then CLK[0..1]_M2C_P/N, are two differential pairs that are assigned for clock signals, which are driven from the IO Mezzanine Module to the carrier card, and, CLK[2..3]_BIDIR_P/N, two differential pairs that are assigned for clock signals, which are driven from the carrier card (DNMEG_HXT) to the IO Mezzanine Module.




The following Rules and Observations are extracts from the FMC specification, reference the ANSI/VITA 57.1 FPGA Mezzanine Card (FMC) Standard for more information:

**Observation 5.11:** CLK0_M2C, CLK1_M2C, are defined in the high-pin count and low-pin count connectors

**Observation 5.12:** CLK2_BIDIR, CLK3_BIDIR, are defined in the high-pin count connector.

**Rule 5.18:** Clocks, CLK0_M2C, CLK1_M2C shall be driven by the IO Mezzanine module and received by the carrier card.

**Rule 5.19:** Clocks, CLK2_BIDIR, CLK3_BIDIR shall be driven by the IO Mezzanine module and received by the carrier card when CLK_DIR is connected to GND or unconnected by the mezzanine module.

**Rule 5.20:** Clocks, CLK2_BIDIR, CLK3_BIDIR shall be driven by the carrier card and received by the IO Mezzanine module when CLK_DIR is connected via a 10K pull up resistor to 3P3V by the mezzanine module.

**Rule 5.21:** CLK[0..3] shall be assigned starting with the lowest ordinal and used in ascending order when CLK_DIR is connected to GND or unconnected..

**Rule 5.22:** CLK[0..1]_M2C shall be assigned to clocks driving from the mezzanine module to the carrier card starting with the lowest ordinal and used in ascending order when CLK_DIR is connected via a 10K pull up resistor to 3P3V by the mezzanine module.

**Rule 5.23:** CLK[2..3]_BIDIR shall be assigned to clocks driving from the carrier card to the mezzanine module starting with the lowest ordinal and used in ascending order when CLK_DIR is connected via a 10K pull up resistor to 3P3V by the mezzanine module.

**Rule 5.24:** CLK[0..3] shall use the LVDS signaling standard.

**Rule 5.25:** All CLK signals shall be connected to differential logical .'0.' By the driving source when not connected to a signal. The .'_P.' signal shall connect to .'0.' and the .'_N.' signal shall connect to '1.'.

**Rule 5.26:** Clock traces shall provide a differential impedance of 100.. +/- 10%

**Rule 5.27:** The differential length mismatch on each differential clock pair shall be a maximum 11ps.

**Rule 5.28:** The maximum period jitter on CLK[0..3] shall be 1ns.

**Rule 5.29:** The maximum cycle to cycle jitter on CLK[0..3] shall be +/- 150ps

**Recommendation 5.5:** CLK[0..1]_M2C (and CLK[2..3]_BIDIR when carrier cards support the configuration of CLK_DIR connected to GND or unconnected) signals should be connected to optimal pins on the FPGA device residing on the carrier card, such as dedicated clock pins.

**Recommendation 5.6:** If a mezzanine module has a need for a particular clock performance, then it should be generated locally on the mezzanine module.

**Rule 5.30:** CLK_DIR shall be implemented as a LVTTL signal

**Rule 5.31:** The Carrier card shall provide a 100K pull-down resister on CLK_DIV signals to GND.

**Rule 5.32:** The Mezzanine module shall connect CLK_DIR to GND or leave unconnected when it is driving a clock on either CLK2_BIDIR or CLK3_BIDIR to the carrier card.

**Rule 5.33:** The Mezzanine module shall connected CLK_DIR via a 10K pull up resistor to 3P3V when it requires the carrier card to drive a clock on either CLK2_BIDIR or CLK3_BIDIR to the mezzanine module

### 3.6.2 Connection between FMC Mezzanine Card Clocks and the FPGA

The connection between the FMC Mezzanine Card clocks and the FPGA are shown in Table 23.

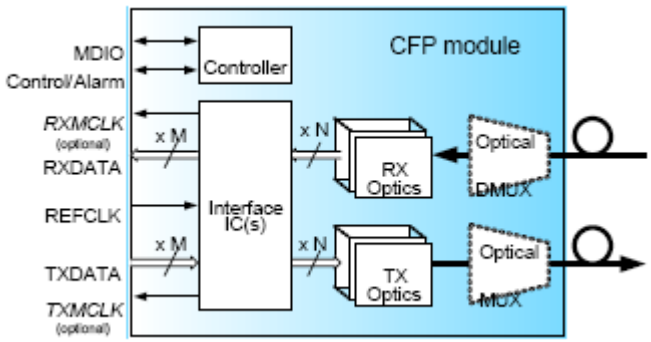
Table 23 - Connections between FMC Mezzanine Card Clocks and the FPGA

| Signal Name | FMC Mezzanine Card | FPGA |
|---|---|---|
| FMC_CLK0_M2C_P | J8-H4 | U34-AR22 |
| FMC_CLK0_M2C_N | J8-H5 | U34-AR21 |
| FMC_CLK1_M2C_P | J8-G2 | U34-R31 |
| FMC_CLK1_M2C_N | J8-G3 | U34-R32 |
| FMC_CLK2_BIDIR_P | J8-K4 | U34-R28 |
| FMC_CLK2_BIDIR_N | J8-K5 | U34-P29 |
| FMC_CLK3_BIDIR_P | J8-J2 | U34-AL22 |
| FMC_CLK3_BIDIR_N | J8-J3 | U34-AM22 |
| FMC_CLK_DIR | J8-B1 | U34-G34 |
| FMC_CLK0_M2C_P | J8-H4 | U34-AR22 |

# 4 High-Speed Interfaces

## 4.1 CFP Interface

One C form-factor pluggable (CFP) interface (J25) is provided on the DNMEG_HXT. The Multi-Source Agreement (MSA) defines the form factor of an optical transceiver which can support 40Gbit/s and 100Gbit/s interfaces for Ethernet, Telecommunications and other applications.

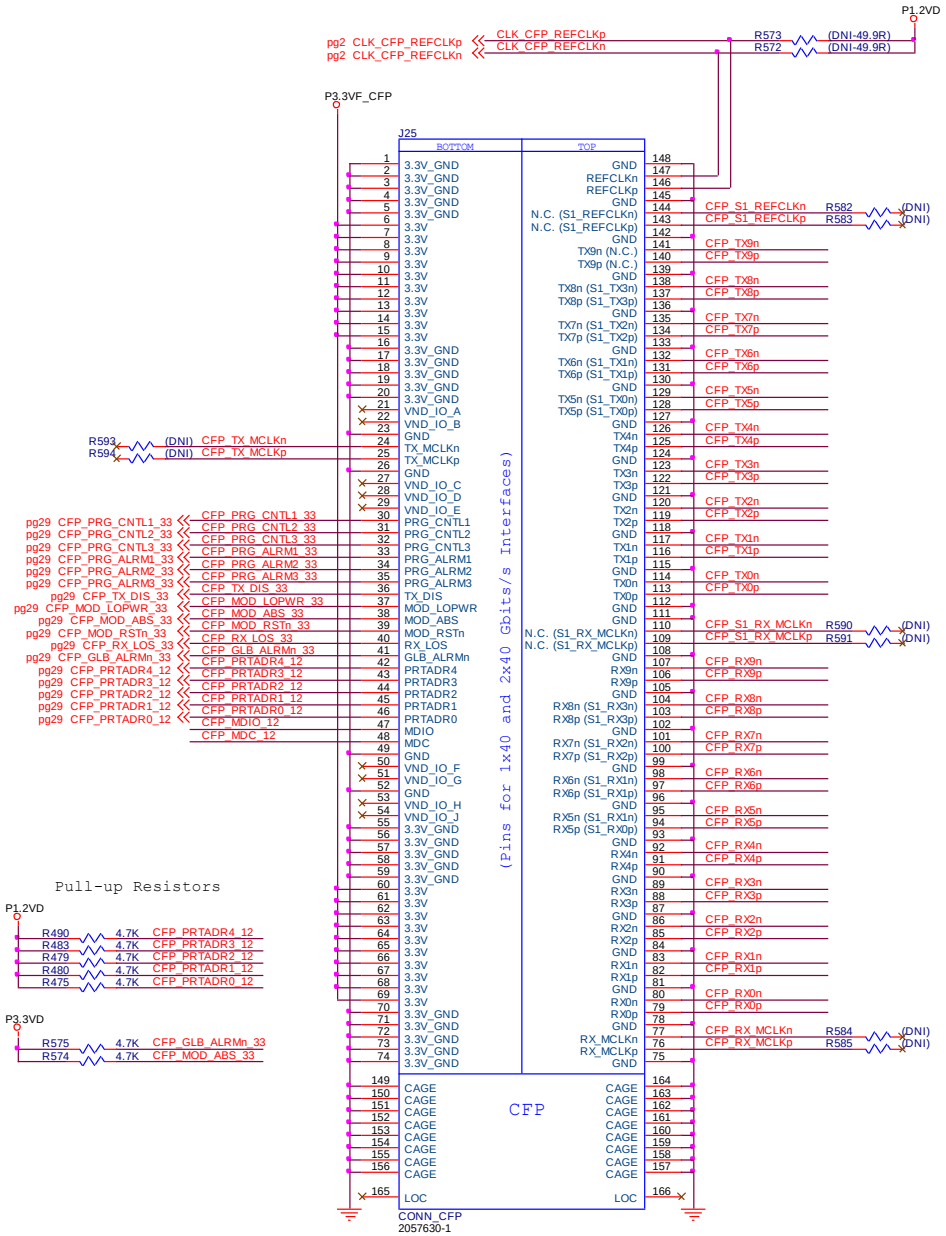



The electrical interface will vary by application, but the nominal signaling lane rate is 10Gbit/s per lane and documentation is provided for CAUI, XLAUI, OTL4.10,

OTL3.4, and STL256.4 electrical interface specifications. The CFP module may be used to support single mode and multimode fiber optics. CFP MSA is an acronym for 100G1 Form factor Pluggable Multi-Source Agreement. For more information reference the CFP MSA Hardware Specification.

### 4.1.1 CFP Circuit

The CFP module and the host system are hot-pluggable. The module or the host system shall not be damaged by insertion or removal of the module. The CFP control signals are routed through the Platform Manager (U33) for level translation from 2.5V to 1.2V. Refer to par 3.2 GTX/GTH Transceiver Clocks for clocking information.



### 4.1.2 Connection between CFP Connector and the FPGA

Table 24 shows the connection between the CFP connector and the FPGA.

Table 24 – Connection between the CFP Connector and the FPGA

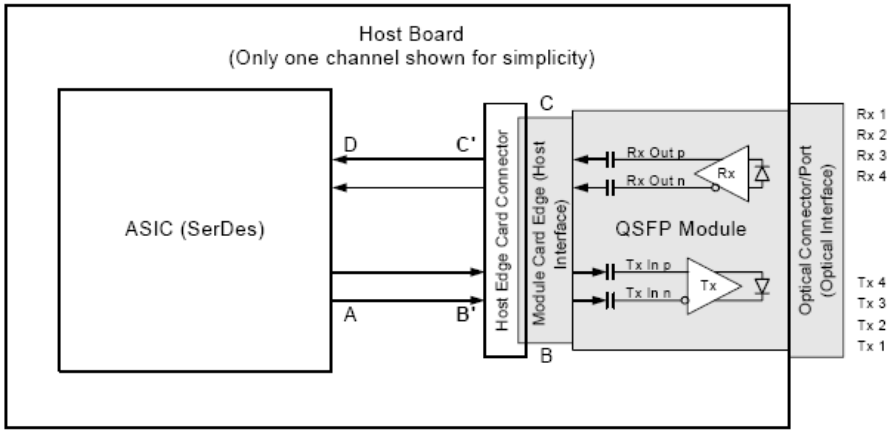
| Signal Name | CFP Connector | FPGA |
|---|---|---|
| CLK_CFP_REFCLKP | J25-146 | U41-15 |
| CLK_CFP_REFCLKN | J25-147 | U41-14 |
| CLK_CFP_MGT106P | U34-R41 | U41-7 |
| CLK_CFP_MGT106N | U34-R42 | U41-6 |
| CLK_CFP_MGT107P | U34-J41 | U41-10 |
| CLK_CFP_MGT107N | U34-J42 | U41-9 |
| CLK_CFP_MGT108P | U34-E41 | U41-12 |
| CLK_CFP_MGT108N | U34-E42 | U41-11 |
| CFP_TX0P | J25-113 | U34-F43 |
| CFP_TX0N | J25-114 | U34-F44 |
| CFP_RX0P | J25-79 | U34-G37 |
| CFP_RX0N | J25-80 | U34-G38 |
| CFP_TX1P | J25-116 | U34-D43 |
| CFP_TX1N | J25-117 | U34-D44 |
| CFP_RX1P | J25-82 | U34-F39 |
| CFP_RX1N | J25-83 | U34-F40 |
| CFP_TX2P | J25-119 | U34-A41 |
| CFP_TX2N | J25-120 | U34-A42 |
| CFP_RX2P | J25-85 | U34-B39 |
| CFP_RX2N | J25-86 | U34-B40 |
| CFP_TX3P | J25-122 | U34-C41 |
| CFP_TX3N | J25-123 | U34-C42 |
| CFP_RX3P | J25-88 | U34-D39 |
| CFP_RX3N | J25-89 | U34-D40 |
| CFP_TX4P | J25-125 | U34-L41 |
| CFP_TX4N | J25-126 | U34-L42 |
| CFP_RX4P | J25-91 | U34-K39 |
| CFP_RX4N | J25-92 | U34-K40 |
| CFP_TX5P | J25-128 | U34-K43 |

| Signal Name | CFP Connector | FPGA |
|---|---|---|
| CFP_TX5N | J25-129 | U34-K44 |
| CFP_RX5P | J25-94 | U34-L37 |
| CFP_RX5N | J25-95 | U34-L38 |
| CFP_TX6P | J25-131 | U34-G41 |
| CFP_TX6N | J25-132 | U34-G42 |
| CFP_RX6P | J25-97 | U34-H39 |
| CFP_RX6N | J25-98 | U34-H40 |
| CFP_TX7P | J25-134 | U34-H43 |
| CFP_TX7N | J25-135 | U34-H44 |
| CFP_RX7P | J25-100 | U34-J37 |
| CFP_RX7N | J25-101 | U34-J38 |
| CFP_TX8P | J25-137 | U34-T43 |
| CFP_TX8N | J25-138 | U34-T44 |
| CFP_RX8P | J25-103 | U34-U41 |
| CFP_RX8N | J25-104 | U34-U42 |
| CFP_TX9P | J25-140 | U34-P43 |
| CFP_TX9N | J25-141 | U34-P44 |
| CFP_RX9P | J25-106 | U34-T39 |
| CFP_RX9N | J25-107 | U34-T40 |
| CFP_PRTADR0 | J25-46 | U34-AL30 |
| CFP_PRTADR1 | J25-45 | U34-BC32 |
| CFP_PRTADR2 | J25-44 | U34-BB32 |
| CFP_PRTADR3 | J25-43 | U34-BA32 |
| CFP_PRTADR4 | J25-42 | U34-AY32 |
| CFP_RX_LOS | J25-40 | U34-AM31 |
| CFP_TX_DIS | J25-36 | U34-BA30 |
| CFP_GLB_ALRMN | J25-41 | U34-AM32 |
| CFP_MOD_ABS | J25-38 | U34-AU31 |
| CFP_MOD_LOPWR | J25-37 | U34-BB30 |
| CFP_MOD_RSTN | J25-39 | U34-AV31 |
| CFP_PRG_ALRM1 | J25-33 | U34-AY31 |
| CFP_PRG_ALRM2 | J25-34 | U34-AJ29 |

| Signal Name | CFP Connector | FPGA |
|---|---|---|
| CFP_PRG_ALRM3 | J25-35 | U34-AK30 |
| CFP_PRG_CNTL1 | J25-30 | U34-AR31 |
| CFP_PRG_CNTL2 | J25-31 | U34-AT32 |
| CFP_PRG_CNTL3 | J25-32 | U34-AW31 |
| CFP_MDC_12 | J25-48 | U34-BD30 |
| CFP_MDIO_12 | J25-47 | U34-AM30 |

## 4.2 QSFP Interface

InfiniBand uses copper CX4 cable for SDR and DDR rates — also commonly used to connect SAS (Serial Attached SCSI) HBAs to external (SAS) disk arrays. With SAS, this is known as an SFF-8470 connector, and is referred to as an "Infiniband style" Connector. The latest connectors used with QDR capable solutions are QSFP (Quad SFP).

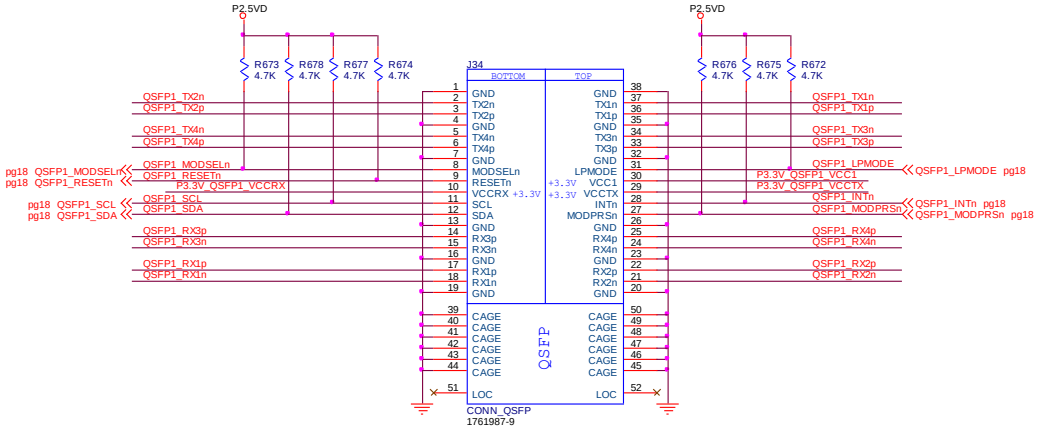



Two QSFP+ (J34, J35) interfaces are provided on the DNMEG_HXT. The electrical and optical specifications are compatible with those enumerated in the ITU-T Recommendation G.957 (STM-1, STM-4 and STM-16), Telcordia Technologies GR-253-CORE (OC-3, OC-12 and OC-48), Ethernet- IEEE 802.3-2005 (Fast Ethernet and Gigabit Ethernet), InfiniBand Architecture Specifications (SDR and DDR) or Fibre Channel-PI-2 (1GFC, 2GFC and 4GFC). Electrical and optical specifications may be compatible with standards under development such as Fibre Channel-PI-3 and Fibre Channel-PI-4. For more information reference the SFF-8436 Specification for the QSFP+ 10Gbs 4X Pluggable Transceiver.

### 4.2.1 QSFP Circuit

The QSFP module and the host system are hot-pluggable. The module or the host system shall not be damaged by insertion or removal of the module. The QSFP control signals are directly connected to the FPGA, while the high-speed signals are connected

directly to the GTH Transceivers. Refer to par 3.2 GTX/GTH Transceiver Clocks for clocking information.




### 4.2.2 Connection between QSFP Connectors and the FPGA

Table 25 shows the connection between the QSFP connectors and the FPGA.

Table 25 – Connection between the QSFP Connector and the FPGA

| Signal Name | QSFP Connector | FPGA |
|---|---|---|
| **Clocking** | | |
| CLK_QSFP_MGT117P | U40-11 | U34-J4 |
| CLK_QSFP_MGT117N | U40-12 | U34-J3 |
| CLK_QSFP_MGT118P | U40-9 | U34-E4 |
| CLK_QSFP_MGT118N | U40-10 | U34-E3 |
| **QSFP 1** | | |
| QSFP1_TX1P | J34-36 | U34-F2 |
| QSFP1_TX1N | J34-37 | U34-F1 |
| QSFP1_RX1P | J34-17 | U34-G8 |
| QSFP1_RX1N | J34-18 | U34-G7 |
| QSFP1_TX2P | J34-3 | U34-D2 |
| QSFP1_TX2N | J34-2 | U34-D1 |
| QSFP1_RX2P | J34-22 | U34-F6 |
| QSFP1_RX2N | J34-21 | U34-F5 |
| QSFP1_TX3P | J34-33 | U34-A4 |
| QSFP1_TX3N | J34-34 | U34-A3 |
| QSFP1_RX3P | J34-14 | U34-B6 |

| Signal Name | QSFP Connector | FPGA |
|---|---|---|
| QSFP1_RX3N | J34-15 | U34-B5 |
| QSFP1_TX4P | J34-6 | U34-C4 |
| QSFP1_TX4N | J34-5 | U34-C3 |
| QSFP1_RX4P | J34-25 | U34-D6 |
| QSFP1_RX4N | J34-24 | U34-D5 |
| QSFP1_INTN | J34-28 | U34-AN31 |
| QSFP1_LPMODE | J34-31 | U34-AN32 |
| QSFP1_MODPRSN | J34-27 | U34-AP31 |
| QSFP1_MODSELN | J34-8 | U34-AR32 |
| QSFP1_RESETN | J34-9 | U34-AJ30 |
| QSFP1_SCL | J34-11 | U34-AU32 |
| QSFP1_SDA | J34-12 | U34-AV32 |
| **QSFP 2** | | |
| QSFP2_TX1P | U34-L4 | J35-36 |
| QSFP2_TX1N | U34-L3 | J35-37 |
| QSFP2_RX1P | U34-K6 | J35-17 |
| QSFP2_RX1N | U34-K5 | J35-18 |
| QSFP2_TX2P | U34-K2 | J35-3 |
| QSFP2_TX2N | U34-K1 | J35-2 |
| QSFP2_RX2P | U34-L8 | J35-22 |
| QSFP2_RX2N | U34-L7 | J35-21 |
| QSFP2_TX3P | U34-G4 | J35-33 |
| QSFP2_TX3N | U34-G3 | J35-34 |
| QSFP2_RX3P | U34-H6 | J35-14 |
| QSFP2_RX3N | U34-H5 | J35-15 |
| QSFP2_TX4P | U34-H2 | J35-6 |
| QSFP2_TX4N | U34-H1 | J35-5 |
| QSFP2_RX4P | U34-J8 | J35-25 |
| QSFP2_RX4N | U34-J7 | J35-24 |
| QSFP2_INTN | J35-28 | U34-AJ31 |
| QSFP2_LPMODE | J35-31 | U34-AT30 |
| QSFP2_MODPRSN | J35-27 | U34-AU30 |

| Signal Name | QSFP Connector | FPGA |
|---|---|---|
| QSFP2_MODSELN | J35-8 | U34-AP30 |
| QSFP2_RESETN | J35-9 | U34-AL32 |
| QSFP2_SCL | J35-11 | U34-AR30 |
| QSFP2_SDA | J35-12 | U34-AK31 |

## 4.3 SFP Interface (up to 6.6Gbps)

The board provides two stacked 2x2 SFP Connectors to allow for 8 channels, connected to GTX Transceivers. The small form-factor pluggable (SFP) is a compact, hot-pluggable transceiver used for both telecommunication and data communications applications. It interfaces a network device mother board (for a switch, router, media converter or similar device) to a fiber optic or copper networking cable. It is a popular industry format supported by many network component vendors. SFP transceivers are designed to support SONET, Gigabit Ethernet, Fibre Channel, and other communications standards.

SFP transceivers are available with a variety of transmitter and receiver types, allowing users to select the appropriate transceiver for each link to provide the required optical reach over the available optical fiber type (e.g. multi-mode fiber or single-mode fiber). Optical SFP modules are commonly available in several different categories:

- 850 nm 550 m multi-mode fiber (SX)
- 1310 nm 10 km single-mode fiber (LX)
- 1490 nm 10 km single-mode fiber (BS-D)
- 1550 nm 40 km (XD), 80 km (ZX), 120 km (EX or EZX)]
- 1490 nm 1310 nm (BX), Single Fiber Bi-Directional Gigabit SFP Transceivers
- DWDM

SFP transceivers are also available with a copper cable interface, allowing a host device designed primarily for optical fiber communications to also communicate over unshielded twisted pair networking cable or transport SDI video signal over coaxial cable. There are also CWDM and single-fiber "bi-directional" (1310/1490 nm Upstream/Downstream) SFPs. SFP transceivers are commercially available with capability for data rates up to 4.25 Gbit/s. An enhanced standard called SFP+ supports data rates up to 10.0 Gbit/s.

Please note the limitation in operating frequency due to Xilinx Virtex-6 clocking limitations, see DS152 - Virtex-6 FPGA Data Sheet - DC and Switching Characteristics for more information:

| Symbol | DC Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{IDIFF}$ | Differential peak-to-peak input voltage | 210 | 800 | 2000 | mV |
| $R_{IN}$ | Differential input resistance | 90 | 100 | 130 | Ω |
| $C_{EXT}$ | Required external AC coupling capacitor | – | 100 | – | nF |

### 4.3.1 SFP Pin Assignments

The SFP pin assignments are listed in Table 26.

Table 26 – SFP Pin Assignments

| Pin Number | Symbol | Description | Logic Family |
|---|---|---|---|
| 1 | VeeT | Transmitter Ground | |
| 2 | TX Fault | Transmitter Fault Indication | LVTTL |
| 3 | TX Disable | Transmitter Disable | |
| 4 | MOD-DEF2 | Module Definition 2 - SDA | |
| 5 | MOD-DEF1 | Module Definition 1 - SCL | |
| 6 | MOD-DEF0 | Module Definition 0 – Module Present | |
| 7 | Rate Sel | LOW or OPEN – reduced bandwidth, HIGH – Full Bandwidth | |
| 8 | LOS | Loss Of Signal | LVTTL |
| 9 | VeeR | Receiver Ground | |
| 10 | VeeR | Receiver Ground | |
| 11 | VeeR | Receiver Ground | |
| 12 | RD- | Inverse Received Data Out | LVPECL |
| 13 | RD+ | Received Data Out | LVPECL |
| 14 | VeeR | Receiver Ground | |
| 15 | VccR | Receiver Power | |
| 16 | VccT | Transmitter Power | |
| 17 | VeeT | Transmitter Ground | |
| 18 | TD+ | Transmitter Data In | LVPECL |
| 19 | TD- | Inverse Transmitter Data In | LVPECL |

| Pin Number | Symbol | Description | Logic Family |
|---|---|---|---|
| 20 | VeeT | Transmitter Ground | |

### 4.3.2 SFP+ Circuit Diagram

SFP connectors (J36, J37) on the DNMEG_HXT are 2x2, medium height press-fit cages, with lightpipes (not used), see Molex P/N 757145001.

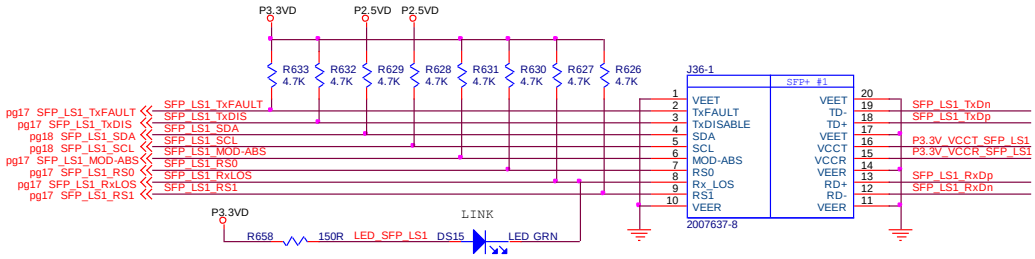



Figure 25 - SFP Interface (channel 1 shown)

Refer to par 3.2 GTX/GTH Transceiver Clocks for clocking information.

### 4.3.3 Connections between 2x2 SFP Connectors and the FPGA

Due to an IO constraint on the FPGA, all the SFP control signals are multiplexed using a CPLD (U53). The $I^2C$ signals are routed point-to-point directly to the FPGA IO Bank 35. Table 27 lists the connections between the 2x2 SFP connectors (J36, J37) and the FPGA (U34).

Table 27 - Connections between 2x2 SFP Connectors and the FPGA

| Signal Name | SFP Connector | FPGA |
|---|---|---|
| **SFP Control Signals – CPLD (U53) to FPGA (U34)** | | |
| CLK_CPLD | U53-32 | U34-BD31 |
| CPLD_R_WN | U53-51 | U34-BC31 |
| RST_CPLD | U53-143 | U34-AW30 |
| SFP_MOD-ABS | U34-F10 | U53-42 |
| SFP_RS0 | U34-E10 | U53-43 |
| SFP_RS1 | U34-D10 | U53-26 |
| SFP_RXLOS | U34-E11 | U53-28 |
| SFP_SEL0 | U34-AY30 | U53-23 |
| SFP_SEL1 | U34-AL29 | U53-22 |
| SFP_SEL2 | U34-AM29 | U53-21 |
| SFP_SEL3 | U34-BB31 | U53-20 |

| Signal Name | SFP Connector | FPGA |
|---|---|---|
| SFP_TXDIS | U34-P10 | U53-41 |
| SFP_TXFAULT | U34-P11 | U53-40 |
| SFP_MOD-ABS | U34-F10 | U53-42 |
| **SFP Control Signals – SFP Connectors to CPLD (U53)** | | |
| SFP_LS1_MOD-ABS | J36-6 | U53-76 |
| SFP_LS1_RS0 | J36-7 | U53-77 |
| SFP_LS1_RS1 | J36-9 | U53-79 |
| SFP_LS1_RXLOS | J36-8 | U53-78 |
| SFP_LS1_SCL | J36-5 | U34-A8 |
| SFP_LS1_SDA | J36-4 | U34-B9 |
| SFP_LS1_TXDIS | J36-3 | U53-75 |
| SFP_LS1_TXFAULT | J36-2 | U53-74 |
| SFP_LS2_MOD-ABS | J36-26 | U53-68 |
| SFP_LS2_RS0 | J36-27 | U53-66 |
| SFP_LS2_RS1 | J36-29 | U53-80 |
| SFP_LS2_RXLOS | J36-28 | U53-64 |
| SFP_LS2_SCL | J36-25 | U34-B12 |
| SFP_LS2_SDA | J36-24 | U34-C13 |
| SFP_LS2_TXDIS | J36-23 | U53-69 |
| SFP_LS2_SDA | J36-24 | U34-C13 |
| SFP_LS2_TXDIS | J36-23 | U53-69 |
| SFP_LS2_TXFAULT | J36-22 | U53-70 |
| SFP_LS3_MOD-ABS | J36-46 | U53-61 |
| SFP_LS3_RS0 | J36-47 | U53-60 |
| SFP_LS3_RS1 | J36-49 | U53-85 |
| SFP_LS3_RXLOS | J36-48 | U53-59 |
| SFP_LS3_SCL | J36-45 | U34-G10 |
| SFP_LS3_SDA | J36-44 | U34-H11 |
| SFP_LS3_TXDIS | J36-43 | U53-83 |
| SFP_LS3_TXFAULT | J36-42 | U53-82 |
| SFP_LS4_MOD-ABS | J36-66 | U53-91 |
| SFP_LS4_RS0 | J36-67 | U53-92 |

| Signal Name | SFP Connector | FPGA |
|---|---|---|
| SFP_LS4_RS1 | J36-69 | U53-57 |
| SFP_LS4_RXLOS | J36-68 | U53-58 |
| SFP_LS4_SCL | J36-65 | U34-A9 |
| SFP_LS4_SDA | J36-64 | U34-B10 |
| SFP_LS4_TXDIS | J36-63 | U53-88 |
| SFP_LS4_TXFAULT | J36-62 | U53-87 |
| SFP_LS5_MOD-ABS | J37-6 | U53-114 |
| SFP_LS5_RS0 | J37-7 | U53-115 |
| SFP_LS5_RS1 | J37-9 | U53-110 |
| SFP_LS5_RXLOS | J37-8 | U53-111 |
| SFP_LS5_SCL | J37-5 | U34-D11 |
| SFP_LS5_SDA | J37-4 | U34-E12 |
| SFP_LS5_TXDIS | J37-3 | U53-113 |
| SFP_LS5_TXFAULT | J37-2 | U53-112 |
| SFP_LS6_MOD-ABS | J37-26 | U53-104 |
| SFP_LS6_RS0 | J37-27 | U53-116 |
| SFP_LS6_RS1 | J37-29 | U53-118 |
| SFP_LS6_RXLOS | J37-28 | U53-117 |
| SFP_LS6_SCL | J37-25 | U34-J11 |
| SFP_LS6_SDA | J37-24 | U34-K11 |
| SFP_LS6_TXDIS | J37-23 | U53-105 |
| SFP_LS6_TXFAULT | J37-22 | U53-106 |
| SFP_LS7_MOD-ABS | J37-46 | U53-102 |
| SFP_LS7_RS0 | J37-47 | U53-101 |
| SFP_LS7_RS1 | J37-49 | U53-121 |
| SFP_LS7_RXLOS | J37-48 | U53-100 |
| SFP_LS7_SCL | J37-45 | U34-F12 |
| SFP_LS7_SDA | J37-44 | U34-G12 |
| SFP_LS7_TXDIS | J37-43 | U53-103 |
| SFP_LS7_TXFAULT | J37-42 | U53-120 |
| SFP_LS8_MOD-ABS | J37-66 | U53-128 |
| SFP_LS8_RS0 | J37-67 | U53-98 |

| Signal Name | SFP Connector | FPGA |
|---|---|---|
| SFP_LS8_RS1 | J37-69 | U53-96 |
| SFP_LS8_RXLOS | J37-68 | U53-97 |
| SFP_LS8_SCL | J37-65 | U34-J10 |
| SFP_LS8_SDA | J37-64 | U34-K10 |
| SFP_LS8_TXDIS | J37-63 | U53-126 |
| SFP_LS8_TXFAULT | J37-62 | U53-125 |
| **GTX - High Speed Interconnect from SFP Connectors to FPGA (U34)** | | |
| SFP_LS1_TXDP | J36-18 | U34-AA3 |
| SFP_LS1_TXDN | J36-19 | U34-AA4 |
| SFP_LS1_RXDP | J36-13 | U34-Y5 |
| SFP_LS1_RXDN | J36-12 | U34-Y6 |
| SFP_LS2_TXDP | J36-38 | U34-Y1 |
| SFP_LS2_TXDN | J36-39 | U34-Y2 |
| SFP_LS2_RXDP | J36-33 | U34-W7 |
| SFP_LS2_RXDN | J36-32 | U34-W8 |
| SFP_LS3_TXDP | J36-58 | U34-W3 |
| SFP_LS3_TXDN | J36-59 | U34-W4 |
| SFP_LS3_RXDP | J36-53 | U34-V5 |
| SFP_LS3_RXDN | J36-52 | U34-V6 |
| SFP_LS4_TXDP | J36-78 | U34-V1 |
| SFP_LS4_TXDN | J36-79 | U34-V2 |
| SFP_LS4_RXDP | J36-73 | U34-U7 |
| SFP_LS4_RXDN | J36-72 | U34-U8 |
| SFP_LS5_TXDP | J37-18 | U34-AE3 |
| SFP_LS5_TXDN | J37-19 | U34-AE4 |
| SFP_LS5_RXDP | J37-13 | U34-AD5 |
| SFP_LS5_RXDN | J37-12 | U34-AD6 |
| SFP_LS6_TXDP | J37-38 | U34-AD1 |
| SFP_LS6_TXDN | J37-39 | U34-AD2 |
| SFP_LS6_RXDP | J37-33 | U34-AC7 |
| SFP_LS6_RXDN | J37-32 | U34-AC8 |
| SFP_LS7_TXDP | J37-58 | U34-AC3 |

| Signal Name | SFP Connector | FPGA |
|---|---|---|
| SFP_LS7_TXDN | J37-59 | U34-AC4 |
| SFP_LS7_RXDP | J37-53 | U34-AB5 |
| SFP_LS7_RXDN | J37-52 | U34-AB6 |
| SFP_LS8_TXDP | J37-78 | U34-AB1 |
| SFP_LS8_TXDN | J37-79 | U34-AB2 |
| SFP_LS8_RXDP | J37-73 | U34-AA7 |
| SFP_LS8_RXDN | J37-72 | U34-AA8 |

## 4.4 SFP+ Interface (up to 11.182Gbps)

The 10GBASE SFP+ modules offer customers a wide variety of 10 Gigabit Ethernet connectivity options for data center, enterprise wiring closet, and service provider transport applications. SFP is defined as Small Form-Factor Pluggable standard by the SFP MSA and is most commonly used for 10 Gigabit Ethernet or 10 Gigabit Fiber Channel applications. The SFP+ modules are hot-pluggable. Hot pluggable refers to plugging in or unplugging a module while the host board is powered. Due to routing losses in the printed circuit board, utilizing 10GSFP+Cu over copper is limited, recommend SFP+ Direct Cable 10GbE Copper, 1.6ft – Amphenol, P/N SF-SFPP2EPASS-000.5.

Please note the limitation in operating frequency due to Xilinx Virtex-6 clocking limitations, see DS152 - Virtex-6 FPGA Data Sheet - DC and Switching Characteristics for more information:

| Symbol | Description | Conditions | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1 | |
| $F_{GTHMAX}$ | Maximum GTH transceiver data rate | PLL Output Divider = 1 | 11.182 | 11.182 | 10.32 | Gb/s |
| | | PLL Output Divider = 4 | 2.795 | 2.795 | 2.58 | Gb/s |
| $F_{GTHMIN}$ | Minimum GTH transceiver data rate(1) | PLL Output Divider = 1 | 9.92 | 9.92 | 9.92 | Gb/s |
| | | PLL Output Divider = 4 | 2.48 | 2.48 | 2.48 | Gb/s |
| $F_{GPLLMAX}$ | Maximum GTH PLL frequency | | 5.591 | 5.591 | 5.16 | GHz |
| $F_{GPLLMIN}$ | Minimum GTH PLL frequency | | 4.96 | 4.96 | 4.96 | GHz |

### 4.4.1 SFP+ Pin Assignments

The SFP+ pin assignments are listed in Table 26.

Table 28 – SFP+ Pin Assignments

| Pin Number | Symbol | Description | Logic Family |
|---|---|---|---|
| 1 | VeeT | Transmitter Ground | |
| 2 | TX Fault | Transmitter Fault Indication | LVTTL-O |

| Pin Number | Symbol | Description | Logic Family |
|---|---|---|---|
| 3 | TX Disable | Transmitter Disable | LVTTL-I |
| 4 | SDA | 2-wire Serial Interface Data Line (Same as MOD-DEF2 in INF-8074i) | LVTTL-I/O |
| 5 | SCL | 2-wire Serial Interface Clock (Same as MOD-DEF1 in INF-8074i) | LVTTL-I/O |
| 6 | Mod_ABS | Module Absent, connected to VeeT or VeeR in the module | |
| 7 | RS0 | Rate Select 0, optionally controls SFP+ module receiver. | LVTTL-I |
| 8 | Rx_LOS | 3rd Receiver Loss of Signal Indication (In FC designated as Rx_LOS and in Ethernet designated as Signal Detect) | LVTTL-O |
| 9 | RS1 | Rate Select 1, optionally controls SFP+ module transmitter | LVTTL-I |
| 10 | VeeR | Receiver Ground | |
| 11 | VeeR | Receiver Ground | |
| 12 | RD- | Inverse Received Data Out | CML-O |
| 13 | RD+ | Received Data Out | CML-O |
| 14 | VeeR | Receiver Ground | |
| 15 | VccR | Receiver Power | |
| 16 | VccT | Transmitter Power | |
| 17 | VeeT | Transmitter Ground | |
| 18 | TD+ | Transmitter Data In | CML-I |
| 19 | TD- | Inverse Transmitter Data In | CML-I |
| 20 | VeeT | Transmitter Ground | |

### 4.4.2 SFP+ Circuit Diagram

SFP+ connectors (J38, J39, J40, and J41) on the DNMEG_HXT are single SFP+ connectors with press-fit heatsinked cages (SAN applications), see Tyco P/N 2007464-2.

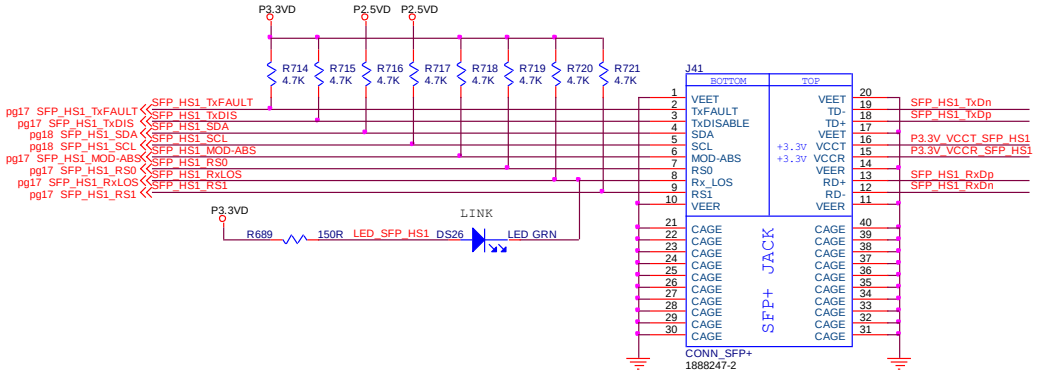



Figure 26 – SFP+ Interface (channel 1 shown)

Refer to par 3.2 GTX/GTH Transceiver Clocks for clocking information.

### 4.4.3 Connections between the SFP+ Connectors and the FPGA

Table 27 lists the connections between the SFP+ connectors (J38, J39, J40 and J41) and the FPGA (U34).

Table 29 - Connections between the SFP+ Connectors and the FPGA

| Signal Name | SFP+ Connector | FPGA |
|---|---|---|
| **SFP+ Clocks (LVPECL)** | | |
| CLK_SFP+HS_MGT116P | U37-9 | U34-R4 |
| CLK_SFP+HS_MGT116N | U37-10 | U34-R3 |
| CLK_SFP+HS_MGT114P_ALT | U37-11 | U34-Y10 |
| CLK_SFP+HS_MGT114N_ALT | U37-12 | U34-Y9 |
| **SFP+ Control** | | |
| SFP_HS1_MOD-ABS | J41-6 | U53-3 |
| SFP_HS1_RS0 | J41-7 | U53-4 |
| SFP_HS1_RS1 | J41-9 | U53-6 |
| SFP_HS1_RXLOS | J41-8 | U53-5 |
| SFP_HS1_SCL | J41-5 | U34-C11 |
| SFP_HS1_SDA | J41-4 | U34-C12 |
| SFP_HS1_TXDIS | J41-3 | U53-2 |
| SFP_HS1_TXFAULT | J41-2 | U53-139 |
| SFP_HS2_MOD-ABS | J40-6 | U53-136 |
| SFP_HS2_RS0 | J40-7 | U53-135 |
| SFP_HS2_RS1 | J40-9 | U53-9 |

| Signal Name | SFP+ Connector | FPGA |
|---|---|---|
| SFP_HS2_RXLOS | J40-8 | U53-134 |
| SFP_HS2_SCL | J40-5 | U34-A12 |
| SFP_HS2_SDA | J40-4 | U34-A13 |
| SFP_HS2_TXDIS | J40-3 | U53-137 |
| SFP_HS2_TXFAULT | J40-2 | U53-138 |
| SFP_HS3_MOD-ABS | J39-6 | U53-133 |
| SFP_HS3_RS0 | J39-7 | U53-132 |
| SFP_HS3_RS1 | J39-9 | U53-130 |
| SFP_HS3_RXLOS | J39-8 | U53-131 |
| SFP_HS3_SCL | J39-5 | U34-A10 |
| SFP_HS3_SDA | J39-4 | U34-B11 |
| SFP_HS3_TXDIS | J39-3 | U53-12 |
| SFP_HS3_TXFAULT | J39-2 | U53-11 |
| SFP_HS4_MOD-ABS | J38-6 | U53-15 |
| SFP_HS4_RS0 | J38-7 | U53-16 |
| SFP_HS4_RS1 | J38-9 | U53-18 |
| SFP_HS4_RXLOS | J38-8 | U53-17 |
| SFP_HS4_SCL | J38-5 | U34-R12 |
| SFP_HS4_SDA | J38-4 | U34-R13 |
| SFP_HS4_TXDIS | J38-3 | U53-14 |
| SFP_HS4_TXFAULT | J38-2 | U53-13 |
| **GTH - High Speed Interconnect from SFP+ Connectors to FPGA (U34)** | | |
| SFP_HS1_TXDP | J41-18 | U34-T2 |
| SFP_HS1_TXDN | J41-19 | U34-T1 |
| SFP_HS1_RXDP | J41-13 | U34-U4 |
| SFP_HS1_RXDN | J41-12 | U34-U3 |
| SFP_HS2_TXDP | J40-18 | U34-P2 |
| SFP_HS2_TXDN | J40-19 | U34-P1 |
| SFP_HS2_RXDP | J40-13 | U34-T6 |
| SFP_HS2_RXDN | J40-12 | U34-T5 |
| SFP_HS3_TXDP | J39-18 | U34-M2 |
| SFP_HS3_TXDN | J39-19 | U34-M1 |

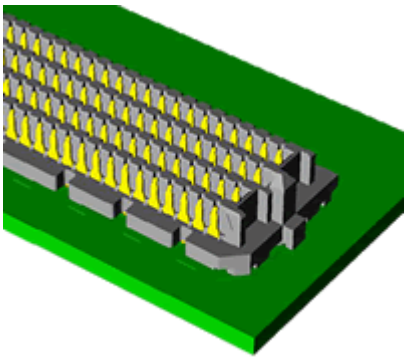
| Signal Name | SFP+ Connector | FPGA |
|---|---|---|
| SFP_HS3_RXDP | J39-13 | U34-N8 |
| SFP_HS3_RXDN | J39-12 | U34-N7 |
| SFP_HS4_TXDP | J38-18 | U34-N4 |
| SFP_HS4_TXDN | J38-19 | U34-N3 |
| SFP_HS4_RXDP | J38-13 | U34-M6 |
| SFP_HS4_RXDN | J38-12 | U34-M5 |

## 4.5 GTX Expansion Interface

A 224-pin, high-speed header, is provided to allow the user access to the GTX Transceiver pairs on the FPGA. The SEAM interface provides 8 differential channels of high-speed serial data to the FPGA. Differential Pair signaling is specified to operate up to 10.5GHz, or 21Gbps, see Samtec Performance Specification. Dini Group provides some daughter cards for this form-factor, currently available is:

- DNSEAM_CX4
- DNSEAM_PCIE
- DNSEAM_SFP

The GTX Expansion Interface could also be used to connect to a custom daughter card.



The board is populated with a Samtec, P/N SEAM-20-03.5-S-08-2-A and mates with a Samtec, P/N SEAF-20-03.5-S-08-2-A on the daughter card.

### 4.5.1 GTX Expansion Circuit Diagram

Eight high-speed differential channels connect directly to the GTX Transceivers on the FPGA (U34). Four REFCLK signals are provided,

CLK_REFCLK_SEAMG_A0/1p/n, and CLK_REFCLK_SEAMG_B0/1p/n, making four independent interfaces on one DNSEAM connection possible. Additionally, for the purpose of control, there are 16 low-speed IO signals that connects to FPGA IO pins, routed as LVDS pairs. A REFCLK is provided for source synchronous applications, SEAMG_IO_D0/1p/n_CC. These signals are routed to clock capable pins on the FPGA. Low-speed IO is fixed at +2.5V signaling levels.

Three voltages are provided to the DNSEAM card, +3.3V, +12V and VCCO. The VCCO supply is fixed at +2.5V, however the daughter card designer should keep in mind that future Dini Boards may choose to supply a different (probably lower) fixed voltage here, such as +1.8V. The diagram below shows the DNSEAM header pin out, see Figure 27.

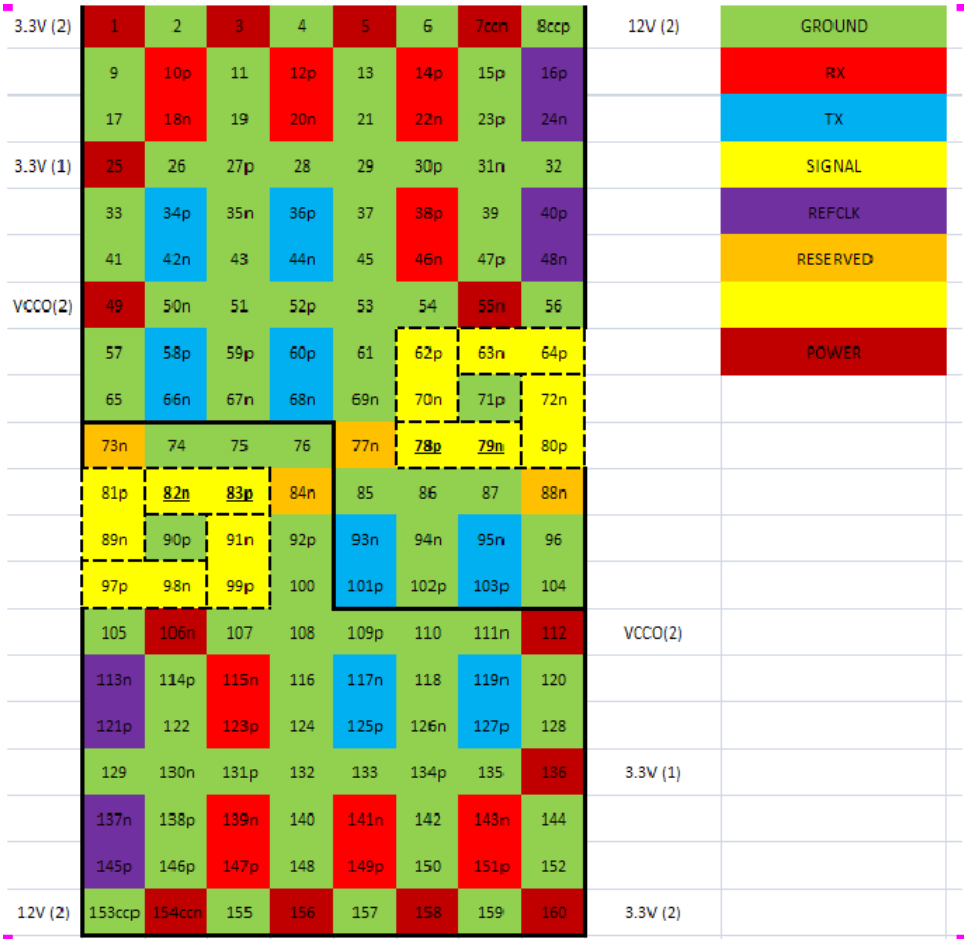



Figure 27 – GTX Expansion Header (SEAM)

### 4.5.2 Connections between FPGA and GTX Expansion Header

Table 30 shows the connections between the FPGA GTX Transceivers and the GTX Expansion header pins.

Table 30 – Connections between FPGA and GTX Expansion Header

| Signal Name | GTX Expansion Header | FPGA |
|---|---|---|
| **Low-Speed IO** | | |
| SEAMG_IO_D0P_CC | J24-78 | U34-P13 |
| SEAMG_IO_D0N_CC | J24-79 | U34-N13 |
| SEAMG_IO_D1P_CC | J24-83 | U34-E15 |
| SEAMG_IO_D1N_CC | J24-82 | U34-D15 |
| SEAMG_IO_D2P | J24-62 | U34-N14 |
| SEAMG_IO_D2N | J24-70 | U34-M14 |
| SEAMG_IO_D3P | J24-64 | U34-H14 |
| SEAMG_IO_D3N | J24-63 | U34-G14 |
| SEAMG_IO_D4P | J24-97 | U34-K13 |
| SEAMG_IO_D4N | J24-98 | U34-J13 |
| SEAMG_IO_D5P | J24-99 | U34-T15 |
| SEAMG_IO_D5N | J24-91 | U34-R15 |
| SEAMG_IO_D6P | J24-80 | U34-M15 |
| SEAMG_IO_D6N | J24-72 | U34-L15 |
| SEAMG_IO_D7P | J24-81 | U34-E13 |
| SEAMG_IO_D7N | J24-89 | U34-D13 |
| **High-Speed IO** | | |
| CLK_REFCLK_SEAMG_A0P | J24-16 | U34-AN8 |
| CLK_REFCLK_SEAMG_A0N | J24-24 | U34-AN7 |
| CLK_REFCLK_SEAMG_A1P | J24-40 | U34-AH10 |
| CLK_REFCLK_SEAMG_A1N | J24-48 | U34-AH9 |
| CLK_REFCLK_SEAMG_B0P | J24-145 | U34-AF10 |
| CLK_REFCLK_SEAMG_B0N | J24-137 | U34-AF9 |
| CLK_REFCLK_SEAMG_B1P | J24-121 | U34-AD10 |
| CLK_REFCLK_SEAMG_B1N | J24-113 | U34-AD9 |
| GTP_SEAMG_TXA0P | J24-34 | U34-AN3 |
| GTP_SEAMG_TXA0N | J24-42 | U34-AN4 |
| GTP_SEAMG_RXA0P | J24-10 | U34-AL7 |
| GTP_SEAMG_RXA0N | J24-18 | U34-AL8 |

| Signal Name | GTX Expansion Header | FPGA |
|---|---|---|
| GTP_SEAMG_TXA1P | J24-36 | U34-AM1 |
| GTP_SEAMG_TXA1N | J24-44 | U34-AM2 |
| GTP_SEAMG_RXA1P | J24-12 | U34-AM5 |
| GTP_SEAMG_RXA1N | J24-20 | U34-AM6 |
| GTP_SEAMG_TXA2P | J24-66 | U34-AL3 |
| GTP_SEAMG_TXA2N | J24-58 | U34-AL4 |
| GTP_SEAMG_RXA2P | J24-14 | U34-AJ7 |
| GTP_SEAMG_RXA2N | J24-22 | U34-AJ8 |
| GTP_SEAMG_TXA3P | J24-68 | U34-AK1 |
| GTP_SEAMG_TXA3N | J24-60 | U34-AK2 |
| GTP_SEAMG_RXA3P | J24-38 | U34-AK5 |
| GTP_SEAMG_RXA3N | J24-46 | U34-AK6 |
| GTP_SEAMG_TXB0P | J24-127 | U34-AJ3 |
| GTP_SEAMG_TXB0N | J24-119 | U34-AJ4 |
| GTP_SEAMG_RXB0P | J24-151 | U34-AH5 |
| GTP_SEAMG_RXB0N | J24-143 | U34-AH6 |
| GTP_SEAMG_TXB1P | J24-125 | U34-AH1 |
| GTP_SEAMG_TXB1N | J24-117 | U34-AH2 |
| GTP_SEAMG_RXB1N | J24-141 | U34-AG8 |
| GTP_SEAMG_RXB1P | J24-149 | U34-AG7 |
| GTP_SEAMG_TXB2P | J24-103 | U34-AG3 |
| GTP_SEAMG_TXB2N | J24-95 | U34-AG4 |
| GTP_SEAMG_RXB2P | J24-147 | U34-AF5 |
| GTP_SEAMG_RXB2N | J24-139 | U34-AF6 |
| GTP_SEAMG_TXB3P | J24-101 | U34-AF1 |
| GTP_SEAMG_TXB3N | J24-93 | U34-AF2 |
| GTP_SEAMG_RXB3P | J24-123 | U34-AE7 |
| GTP_SEAMG_RXB3N | J24-115 | U34-AE8 |

## 4.6 SATA II Interface

Serial ATA (SATA or Serial Advanced Technology Attachment) is a computer bus interface for connecting host bus adapters to mass storage devices such as hard disk drives and optical drives. Serial ATA was designed to replace the older ATA (AT

Attachment) standard (also known as EIDE), offering several advantages over the older parallel ATA (PATA) interface: reduced cable-bulk and cost (7 conductors versus 40), native hot swapping, faster data transfer through higher signaling rates, and more efficient transfer through an (optional) I/O queuing protocol.

SATA host-adapters and devices communicate via a high-speed serial cable over two pairs of conductors. To ensure backward compatibility with legacy ATA software and applications, SATA uses the same basic ATA and ATAPI command-set as legacy ATA devices.

### 4.6.1 SATA II Circuit Diagram

The SATA II interfaces are hardwired for HOST/DEVICE operation. Both TX/RX signal pairs are differentially routed and AC-coupled with 0.1uF capacitors, see Figure 28.

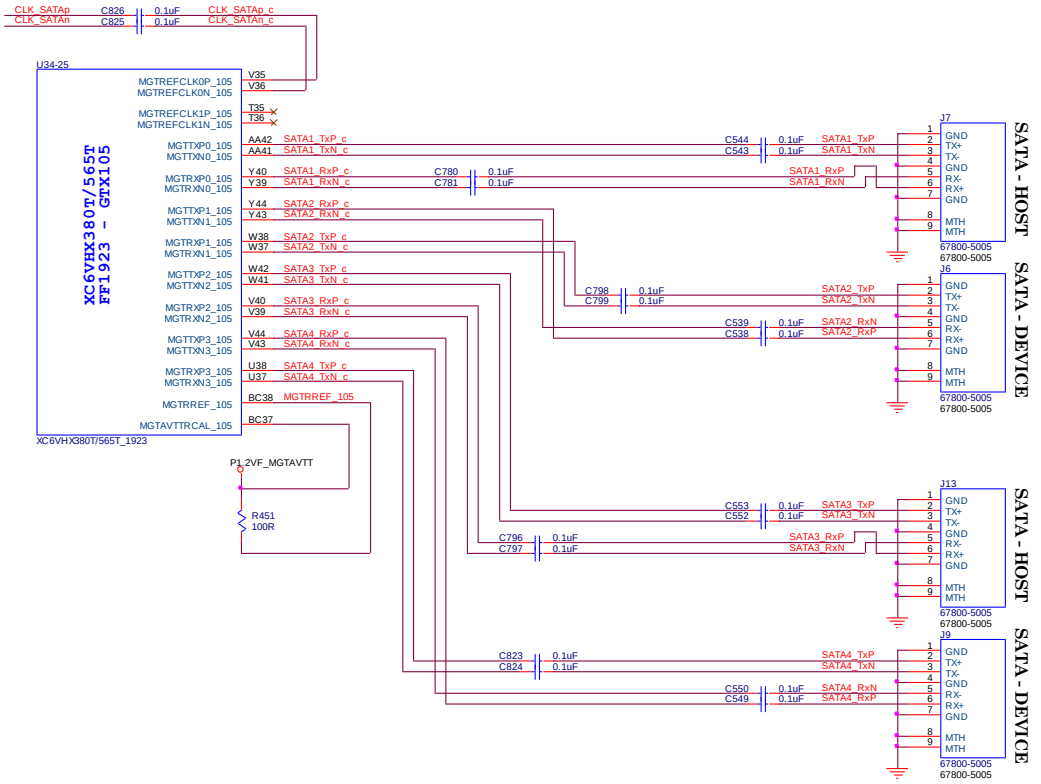



Figure 28 - SATA II Interface

LVDS Oscillator (X2) is AC-Coupled to the GTX Transceiver clock inputs on the FPGA. Note: The frequency select signals of the oscillator are connected to the FPGA, and hardwired using discrete resistors (R458/R468). The default factory installed oscillator is running at 150MHz (fixed). They are available from Nu Horizons, Pletronics P/N LV7745DW-150.0M. The oscillator power supply is filtered to reduce power

supply noise and jitter. Please see the LV7745DW-150.0M datasheet for more information.

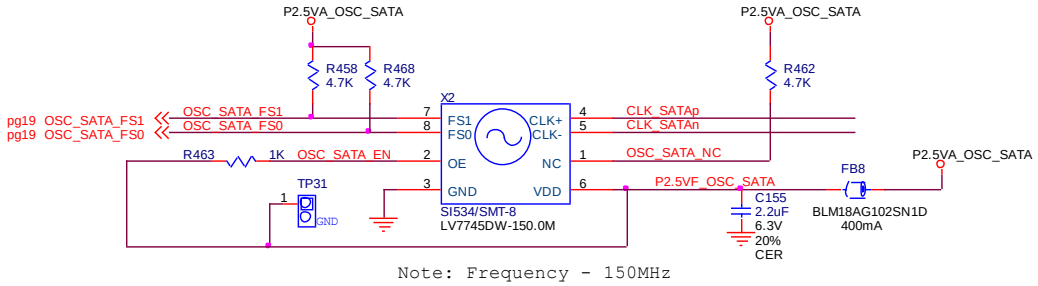



Figure 29 – SATA II GTX Oscillator

### 4.6.2 Connections between FPGA and SATA II Connectors

Table 31 shows the connections between the FPGA GTX Transceivers and the SATA II connector pins.

Table 31 – Connections between FPGA and SATA II Connectors/Oscillator

| Signal Name | OSC/SATA | FPGA |
|---|---|---|
| **SATA Clock** | | |
| CLK_SATAP | X2-4 | U34-V35 |
| CLK_SATAN | X2-5 | U34-V36 |
| OSC_SATA_FS0 | X2-8 | U34-AN34 |
| OSC_SATA_FS1 | X2-7 | U34-AM34 |
| **SATA 1 – HOST (MGT105)** | | |
| SATA1_TXP | J7-2 | U34-AA42 |
| SATA1_TXN | J7-3 | U34-AA41 |
| SATA1_RXP | J7-6 | U34-Y40 |
| SATA1_RXN | J7-5 | U34-Y39 |
| **SATA 2 – DEVICE (MGT105)** | | |
| SATA2_TXP | J6-2 | U34-W38 |
| SATA2_TXN | J6-3 | U34-W37 |
| SATA2_RXP | J6-6 | U34-Y44 |
| SATA2_RXN | J6-5 | U34-Y43 |
| **SATA 3 – HOST (MGT105)** | | |
| SATA3_TXP | J13-2 | U34-W42 |
| SATA3_TXN | J13-3 | U34-W41 |

| Signal Name | OSC/SATA | FPGA |
|---|---|---|
| SATA3_RXP | J13-6 | U34-V40 |
| SATA3_RXN | J13-5 | U34-V39 |
| **SATA 4 – DEVICE (MGT105)** | | |
| SATA4_TXP | J9-2 | U34-U38 |
| SATA4_TXN | J9-3 | U34-U37 |
| SATA4_RXP | J9-6 | U34-V44 |
| SATA4_RXN | J9-5 | U34-V43 |

## 4.7 PCI Express Cable

One iPass connector (x4), configured for PCI Express (DownStream), and one iPass connector (x4), configured for PCI Express (UpStream) is connected to the FPGA. The PCI Express External Cabling specification establishes a standard method of using PCI Express technology over a cable by defining cable connectors, copper cabling attributes and electrical characteristics, connector retention, identification and labeling. The board conforms to the PCI Express External Cabling Specification Revision 1.0, enabling high data rates (2.5Gb/s) between PCI Express subsystems. Standard cables and connectors have been defined for x1, x4, x8, and x16 link widths. Sideband signaling is provided via the cable to attain compatibility with existing silicon and software; this leverages existing software and infrastructure, provides ease-of-use and helps accelerate adoption of the technology. See *PCI Express External Cabling Specification Rev 1.0* available from PCI-SIG for more information.

The PCI Express Cable Connector supports the following Auxiliary signals:

- CREFCLKp/CREFCLKn (required): Low voltage differential cable reference clock.
- CPRSNTn (required): Cable present detect, an active-low signal provided by a Downstream Subsystem to indicate that it's both present and its power is "good" (within tolerance).
- CPERSTn (required): Cable PERST#, an active-low signal, logically equivalent to system PERSTn (platform reset), driven by the Upstream Subsystem.
- CPWRON (required): Cable Power On, an active-high signal provided by an Upstream Subsystem to notify slave-type Downstream Subsystems to turn their main power on or off, used for example to put a slave Subsystem into the S3 power management state.

- SB_RTN (required): The SideBand Return provides a return current path for all single ended sideband signals, allowing for power domain isolation between Subsystems.

- CWAKEn (required): Cable Wake, an active-low signal that is driven by a Downstream Subsystem to re-activate the PCI Express hierarchy's main power rails and reference clocks. Although optional for Upstream and Downstream Subsystems, all cable assemblies shall include CWAKEn. It is required on any Subsystem that supports wakeup functionality compliant with the specification.

- +3.3 V POWER (optional for connector): Power provisioning to the connector backshell is provided to allow for active signal conditioning components within the cable assembly. A wire shall not be provided within the cable.

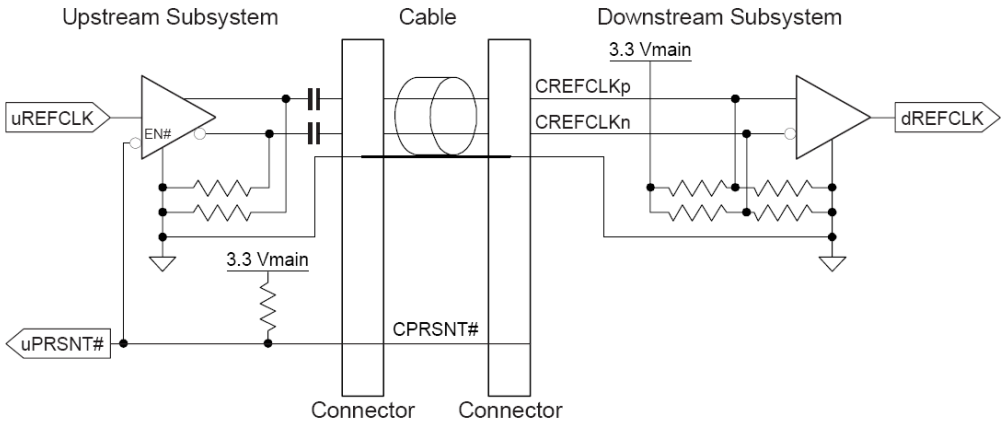
- PWR_RTN (optional for connector): Return path optional for +3.3 V power provisioning.

### 4.7.1 Cable Reference Clocking Options

To control jitter, radiated emissions, and crosstalk, and allow for future silicon fabrication process changes, a low voltage swing, current mode, differential clock is specified. Isolated power domains, between the two Subsystems, are maintained through implementation of AC-coupling capacitors at the source. Supplying the cable reference clock is required from an Upstream Subsystem.

- Downstream Device, Clock from remote REFCLK on cable

- Downstream Device, Clock from local PCI Express Clock Buffer (U24)




### 4.7.2 Cable Present

"Power Good" signaling is accomplished with the following signals: PCIE_CPERSTn / PCIE_CPWRON, for signaling the status of the Upstream Subsystem, and PCIE_CPRSNTn as described within this section. PCIE_CPRSNTn assertion by the

Downstream Subsystem is qualified by the power good condition of the Downstream Subsystem, as illustrated in Figure 30. This provides a mechanism for the Upstream Subsystem to determine whether the power is good within the Downstream Subsystem, enable the reference clock, and initiate Link Training.

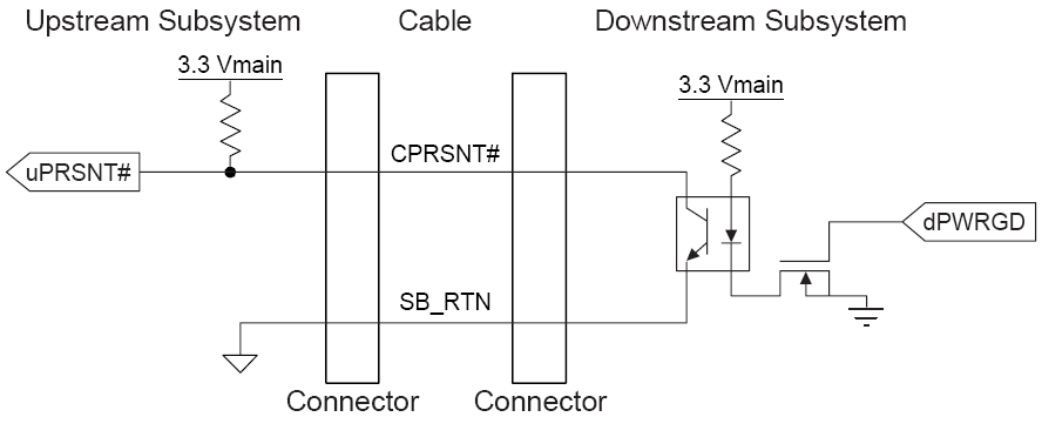



Figure 30 – CPRSNT# Signaling with Power Isolation

Opto-couplers (U8, U9) provide power isolation between the Upstream and the Downstream system. Note: PCIEx_FPGA_CPERSTn/ PCIEx_FPGA_CPWRON is an active LOW signal in "To Slave (Upstream)" mode and an active HIGH signal when in "From Host (Downstream)" mode. Refer to par 3.3 PCI Express Cable Reference Clocks (HCSL) for clocking information.

### 4.7.3 Connections between FPGA and the PCI Express Cable Connector

Table 32 lists the connections between the high-speed serial transceivers (GTX) on the FPGA and the PCI Express connector. Note: Tx Pairs are isolated by 0.1uF ceramic capacitors.

Table 32 - Connections between FPGA and the PCI Express Cable Connector

| Signal Name | PCI Express Cable | FPGA |
|---|---|---|
| PCIE1_RECLKP | J4-A14 | Multiple Sources, see Schematic |
| PCIE1_RECLKN | J4-A15 | Multiple Sources, see Schematic |
| PCIE1_PETP0 | J4-A2 | U34-AE42 |
| PCIE1_PETN0 | J4-A3 | U34-AE41 |
| PCIE1_PERP0 | J4-B2 | U34-AD40 |
| PCIE1_PERN0 | J4-B3 | U34-AD39 |

| Signal Name | PCI Express Cable | FPGA |
|---|---|---|
| PCIE1_PETP1 | J4-A5 | U34-AD44 |
| PCIE1_PETN1 | J4-A6 | U34-AD43 |
| PCIE1_PERP1 | J4-B5 | U34-AC38 |
| PCIE1_PERN1 | J4-B6 | U34-AC37 |
| PCIE1_PETP2 | J4-A8 | U34-AC42 |
| PCIE1_PETN2 | J4-A9 | U34-AC41 |
| PCIE1_PERP2 | J4-B8 | U34-AB40 |
| PCIE1_PERN2 | J4-B9 | U34-AB39 |
| PCIE1_PETP3 | J4-A11 | U34-AB44 |
| PCIE1_PETN3 | J4-A12 | U34-AB43 |
| PCIE1_PERP3 | J4-B11 | U34-AA38 |
| PCIE1_PERN3 | J4-B12 | U34-AA37 |
| PCIE1_FPGA_CPERSTN | U7-6/S1-5 | U34-A15 |
| PCIE1_FPGA_CPWRON | U7-7/S1-6 | U34-B15 |
| PCIE1_FPGA_CPRSNT | U6-1/S1-1 | U34-B17 |
| PCIE1_FPGA_CWAKE | U6-3/S1-2 | U34-A17 |
| PCIE2_RECLKP | J5-A14 | Multiple Sources, see Schematic |
| PCIE2_RECLKN | J5-A15 | Multiple Sources, see Schematic |
| PCIE2_PETP0 | J5-A2 | U34-AJ42 |
| PCIE2_PETN0 | J5-A3 | U34-AJ41 |
| PCIE2_PERP0 | J5-B2 | U34-AH40 |
| PCIE2_PERN0 | J5-B3 | U34-AH39 |
| PCIE2_PETP1 | J5-A5 | U34-AH44 |
| PCIE2_PETN1 | J5-A6 | U34-AH43 |
| PCIE2_PERP1 | J5-B5 | U34-AG38 |
| PCIE2_PERN1 | J5-B6 | U34-AG37 |
| PCIE2_PETP2 | J5-A8 | U34-AG42 |
| PCIE2_PETN2 | J5-A9 | U34-AG41 |
| PCIE2_PERP2 | J5-B8 | U34-AF40 |
| PCIE2_PERN2 | J5-B9 | U34-AF39 |
| PCIE2_PETP3 | J5-A11 | U34-AF44 |

| Signal Name | PCI Express Cable | FPGA |
|---|---|---|
| PCIE2_PETN3 | J5-A12 | U34-AF43 |
| PCIE2_PERP3 | J5-B11 | U34-AE38 |
| PCIE2_PERN3 | J5-B12 | U34-AE37 |
| PCIE2_FPGA_CPERSTN | U9-6/S2-5 | U34-F15 |
| PCIE2_FPGA_CPWRON | U9-7/S2-6 | U34-G15 |
| PCIE2_FPGA_CPRSNT | U8-1/S2-1 | U34-C16 |
| PCIE2_FPGA_CWAKE | U8-3/S2-2 | U34-B16 |

# 5 LED Indicators

The DNMEG_V6HXT Logic Emulation board provides various LED's to indicate that status of the board. The LEDs are turned ON by driving the GATE of the N-MOSFET HIGH, see Figure 31.

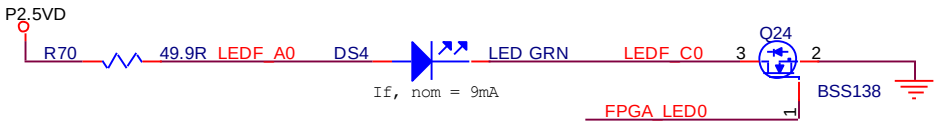



Figure 31 - LED Indicator

## 5.1 FPGA Status LEDs

Numerous LEDs (Green) are provided to the user as a design aid during debugging. The LEDs can be turned ON by driving the corresponding pin HIGH. Table 33 describes the Status LEDs and their associated pin assignments on the FPGA.

Table 33 – FPGA Status LEDs

| Signal Name | FPGA | LED |
|---|---|---|
| FPGA_LED0 | U34-BD34 | LED0 (DS4) |
| FPGA_LED1 | U34-BD35 | LED1 (DS3) |
| FPGA_LED2 | U34-BA33 | LED2 (DS2) |
| FPGA_LED3 | U34-BA34 | LED3 (DS1) |

## 5.2 Configuration DONE LEDs

After the FPGA have received all the configuration data successfully, it releases the DONE pin, which is pulled high by a pull-up resistor. A low-to-high transition on the DONE indicates configuration is complete and initialization of the device can begin. DONE pin drives an N-MOSFET and turns ON a blue LED when the DONE pin

goes high. Table 34 describes the DONE LED and its associated pin assignment on the FPGA.

Table 34 – FPGA DONE LED

| Signal Name | FPGA | LED |
|---|---|---|
| FPGA_DONE | U34-T13 | DS5 |

## 5.3 Platform Manager Status LEDs

Numerous LEDs (Green) are provided to the user as a design aid during debugging. The LEDs can be turned ON by driving the corresponding pin HIGH. Table 33 describes the Status LEDs and their associated pin assignments on the Platform Manager.

Table 35 – CPLD Status LEDs

| Signal Name | PLTFRM MNGR | LED |
|---|---|---|
| CPLD_LED0 | U33-R12 | LED0 (DS6) |
| CPLD_LED1 | U33-P10 | LED1 (DS8) |
| CPLD_LED2 | U33-T13 | LED2 (DS10) |
| CPLD_LED3 | U33-P11 | LED3 (DS12) |
| CPLD_LED_RST | U33-T14 | RST SYS (DS13) |

Note: LED[3..0] is intended to indicate PSU failed and also provides a heart-beat LED for the Power Monitor.

## 5.4 USB Fault LED

The AP2171 is an integrated high-side power switch optimized for Universal Serial Bus (USB) and other hot-swap applications. The device complies with USB 2.0 and offer current and thermal limiting, including short circuit protection as well as controlled rise time and under-voltage lockout functionality. A 7ms deglitch capability on the open-drain Flag output prevents false over-current reporting and will turn on LED (DS27) during an over-current condition, see Table 36.

Table 36 – USB Fault LED

| Signal Name | Source Pin | LED |
|---|---|---|
| USB0_OCn | U56-5 | USB OC (DS27) |

## 5.5 Miscellaneous LEDs

Table 37 describes the miscellaneous status LEDs and their associated source.

Table 37 – Miscellaneous LEDs

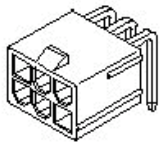
| Signal Name | Source | LED |
|---|---|---|
| **CPU LEDs (U26)** | | |
| MCU_RSTOUTn | U26-11 | RST OUT (DS11) |
| MCU_HRTBEAT | U26-65 | HRT BT (DS7) |
| USB_UP_LED | U26-25 | USB UP (DS9) |
| **MGT Clock Generator – LOL Indicator** | | |
| MGT_INTR | U47-8 | LOL (DS14) |
| **SFP+ - LOS Indictors** | | |
| SFP_LS1_RXLOS | U53-78 | SFP+ LOS (DS15) |
| SFP_LS2_RXLOS | U53-64 | SFP+ LOS (DS16) |
| SFP_LS3_RXLOS | U53-59 | SFP+ LOS (DS17) |
| SFP_LS4_RXLOS | U53-59 | SFP+ LOS (DS18) |
| SFP_LS5_RXLOS | U53-111 | SFP+ LOS (DS19) |
| SFP_LS6_RXLOS | U53-117 | SFP+ LOS (DS20) |
| SFP_LS7_RXLOS | U53-100 | SFP+ LOS (DS21) |
| SFP_LS8_RXLOS | U53-97 | SFP+ LOS (DS22) |
| SFP_HS1_RxLOS | U53-5 | SFP+ LOS (DS26) |
| SFP_HS2_RxLOS | U53-134 | SFP+ LOS (DS25) |
| SFP_HS3_RxLOS | U53-131 | SFP+ LOS (DS24) |
| SFP_HS4_RxLOS | U53-17 | SFP+ LOS (DS23) |
| **Front Panel PWR LED** | | |
| PWR_OK | J3-8 | ATX PWR OK (DS28) |

# 6 Power Distribution

The DNMEG_V6HXT Logic Emulation Board supports a wide range of technologies, from legacy devices like serial ports, to DDR3 SDRAM, Optical Interfaces and Transceivers on the Xilinx FPGA. This wide range of technologies, including the various FPGA power supplies requires a variety of power supplies. These are provided on the DNMEG_V6HXT Logic Emulation Board using a combination of switching and linear power regulators.

## 6.1 Stand Alone Operation

An external ATX power supply is used to supply power to the DNMEG_V6HXT Logic Emulation Board in stand-alone mode, see Figure 33. The external power supply connects to a "24-Pin Mini-Fit Jr. ATX Power" header (J3), Molex P/N 39-29-1248.



The user should connect the matching male power connector on the ATX power supply to this header. The DNMEG_V6HXT Logic Emulation Board has the following shared power supplies; they are generated from the +12V supply on the external power connector (J3). In addition, P5.0V_ATX and P3.3V_ATX are also used to drive LDO supplies etc.

| Power Supply | Source |
|---|---|
| P12V_ATX | J3-10, 11 |
| P2.5VD | PSU2-2,3 |
| P3.3VD | PSU3-5 |
| P5.0V | PSU6-2, 3 |
| P_FMC_VADJ | PSU1-4 |
| P1.0V_VCCINT | PSU4-10, 11 |
| P2.5VA_DCA_LIM | U10-1 |
| P_DIMM | PSU8-4 |

Dini Group recommends a power supply rated for 750W, see Antec EarthWatts Series EA-750, P/N N82E16817371051.

Figure 32 - ATX Power Supply

### 6.1.1 External Power Connector

Figure 33 indicates the connections to the external power connector (J3). This header is fully polarized to prevent reverse connection and is rated for 600VAC at 6A per contact. Jumper (J33) must be installed for the ATX Power Supply to turn ON.

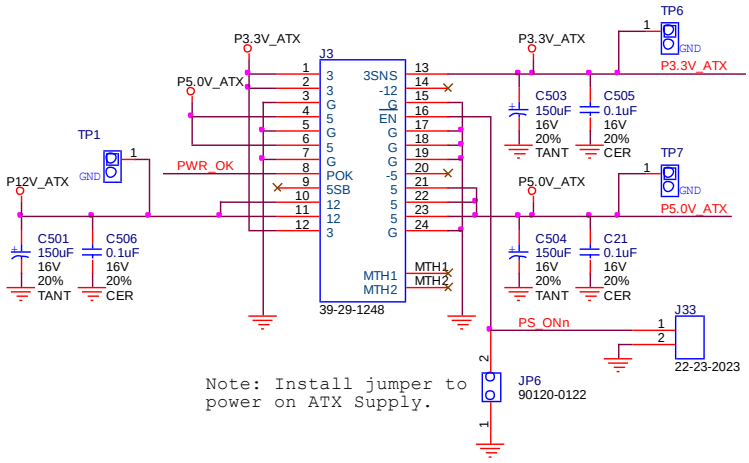



Figure 33 - External Power Connection

Note: Header J3 is not hot-plug able. Do not attach power while power supply is ON.

## 6.2 Voltage Monitors and Reset

The Lattice Platform Manager (LPTM10-12107) integrates board power management (hot-swap, sequencing, monitoring, reset generation, trimming and margining) and digital board management functions (reset tree, non-volatile error logging, glue logic, board digital signal monitoring and control, system bus interface, etc.) into a single integrated solution. The Platform Manager provides 12 independent analog input channels to monitor 12 power supplies. Up to six general purpose 5V tolerant digital inputs are also provided for miscellaneous control functions. There are 16 open-drain digital outputs that can be used for controlling DC-DC converters, low-drop-out regulators (LDOs) and opto-couplers, as well as for supervisory and general purpose logic interface functions.

### 6.2.1 Power Sequencing

The Virtex-6 FPGAs have power-up requirements; refer to the datasheet for the requirements. Power sequencing is implemented by the Platform Manager (U33).

### 6.2.2 Reset Options

A Logic (S4) reset from the Platform Manager (U33) is directly connected to the FPGA, see Table 38. The System (S5) reset, powers down the power supplies and generates a power ON/OFF reset to the board. The Platform Manager holds the MCU (U26) in RESET until the power supplies are up and stable.

Table 38 – Logic Reset for the FPGA

| Signal Name | Platform Manager | FPGA / MCU |
|---|---|---|
| RST_CPLD_LOGN (S4) | U33-T11 | U34-BC34 |
| MCU_RSTN | U33-R11 | U26-14 |

# 7 FMC Mezzanine Card

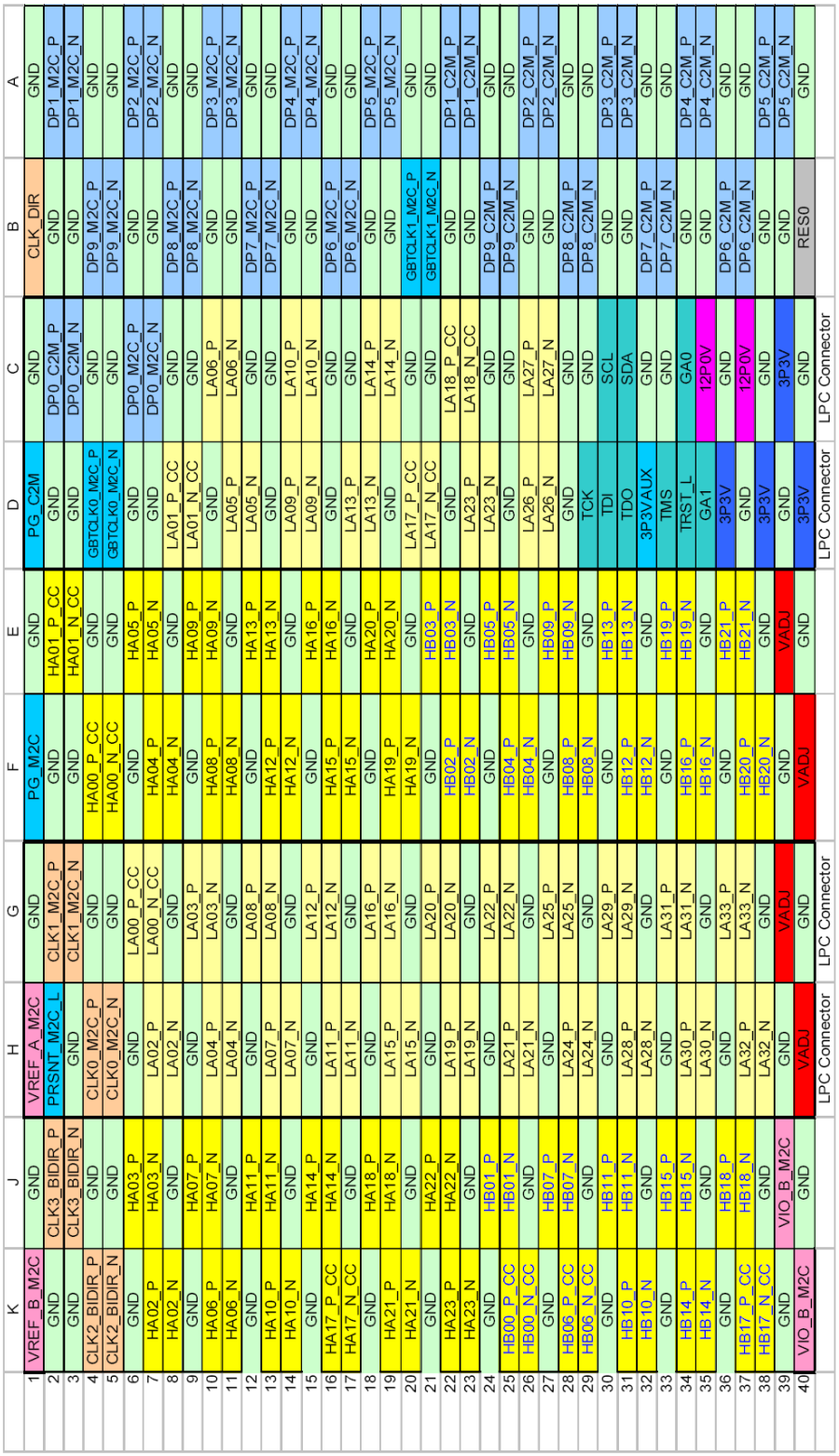
The FMC (also known as VITA 57) standard was developed to provide an industry standard mezzanine form factor in support of a flexible, modular IO interface to an FPGA located on a baseboard or carrier card. It allows the physical IO interface to be decoupled from the FPGA design while maintaining a close coupling between a physical IO interface and an FPGA.

## 7.1 FMC Clocking

A High Pin Count (HPC), single-width (69 mm x 76.5 mm), FMC connector (J8) with 400 pins is provided on the board. Refer to par 3.6 FMC Mezzanine Card Clocks for clocking information.

## 7.2 FMC Pin Assignments

Refer to the FMC Specification AV57DOT1 - R2010 for more information pin assignments.



| | K | J | H | G | F | E | D | C | B | A |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | VREF_B_M2C | GND | VREF_A_M2C | GND | PG_M2C | GND | PG_C2M | GND | CLK_DIR | GND |
| 2 | GND | CLK3_BIDIR_P | PRSNT_M2C_L | CLK1_M2C_P | GND | HA01_P_CC | GND | DP0_C2M_P | GND | DP1_M2C_P |
| 3 | GND | CLK3_BIDIR_N | GND | CLK1_M2C_N | GND | HA01_N_CC | GND | DP0_C2M_N | GND | DP1_M2C_N |
| 4 | CLK2_BIDIR_P | GND | CLK0_M2C_P | GND | HA00_P_CC | GND | GBTCLK0_M2C_P | GND | DP9_M2C_P | GND |
| 5 | CLK2_BIDIR_N | GND | CLK0_M2C_N | GND | HA00_N_CC | GND | GBTCLK0_M2C_N | GND | DP9_M2C_N | GND |
| 6 | GND | HA03_P | GND | LA00_P_CC | GND | HA05_P | GND | DP0_M2C_P | GND | DP2_M2C_P |
| 7 | HA02_P | HA03_N | LA02_P | LA00_N_CC | HA04_P | HA05_N | GND | DP0_M2C_N | GND | DP2_M2C_N |
| 8 | HA02_N | GND | LA02_N | GND | HA04_N | GND | LA01_P_CC | GND | DP8_M2C_P | GND |
| 9 | GND | HA07_P | GND | LA03_P | GND | HA09_P | LA01_N_CC | GND | DP8_M2C_N | GND |
| 10 | HA06_P | HA07_N | LA04_P | LA03_N | HA08_P | HA09_N | GND | LA06_P | GND | DP3_M2C_P |
| 11 | HA06_N | GND | LA04_N | GND | HA08_N | GND | LA05_P | LA06_N | GND | DP3_M2C_N |
| 12 | GND | HA11_P | GND | LA08_P | GND | HA13_P | LA05_N | GND | DP7_M2C_P | GND |
| 13 | HA10_P | HA11_N | LA07_P | LA08_N | HA12_P | HA13_N | GND | LA10_P | DP7_M2C_N | GND |
| 14 | HA10_N | HA14_P | LA07_N | GND | HA12_N | GND | LA09_P | LA10_N | GND | DP4_M2C_P |
| 15 | GND | HA14_N | GND | LA12_P | GND | HA16_P | LA09_N | GND | DP6_M2C_P | DP4_M2C_N |
| 16 | HA17_P_CC | HA14_N | LA11_P | LA12_N | HA15_P | HA16_N | GND | GND | DP6_M2C_N | GND |
| 17 | HA17_N_CC | GND | LA11_N | GND | HA15_N | GND | LA13_P | GND | GND | GND |
| 18 | GND | HA18_P | GND | LA16_P | GND | HA20_P | LA13_N | LA14_P | DP5_M2C_P | DP5_M2C_N |
| 19 | HA21_P | HA18_N | LA15_P | LA16_N | HA19_P | HA20_N | GND | LA14_N | GND | GND |
| 20 | HA21_N | GND | LA15_N | GND | HA19_N | GND | LA17_P_CC | GND | GBTCLK1_M2C_P | GND |
| 21 | GND | HA22_P | GND | LA20_P | GND | HB03_P | LA17_N_CC | GND | GBTCLK1_M2C_N | GND |
| 22 | HA23_P | HA22_N | LA19_P | LA20_N | HB02_P | HB03_N | GND | LA18_P_CC | GND | DP1_C2M_P |
| 23 | HA23_N | GND | LA19_N | GND | HB02_N | GND | LA23_P | LA18_N_CC | GND | DP1_C2M_N |
| 24 | GND | HB01_P | GND | LA22_P | GND | HB05_P | LA23_N | GND | DP9_C2M_P | GND |
| 25 | HB00_P_CC | HB01_N | LA21_P | LA22_N | HB04_P | HB05_N | GND | GND | DP9_C2M_N | GND |
| 26 | HB00_N_CC | GND | LA21_N | GND | HB04_N | GND | LA26_P | LA27_P | GND | DP2_C2M_P |
| 27 | GND | HB07_P | GND | LA25_P | GND | HB09_P | LA26_N | LA27_N | GND | DP2_C2M_N |
| 28 | HB06_P_CC | HB07_N | LA24_P | LA25_N | HB08_P | HB09_N | GND | GND | DP8_C2M_P | GND |
| 29 | HB06_N_CC | GND | LA24_N | GND | HB08_N | GND | TCK | GND | DP8_C2M_N | GND |
| 30 | GND | HB11_P | GND | LA29_P | GND | HB13_P | TDI | SCL | GND | DP3_C2M_P |
| 31 | HB10_P | HB11_N | LA28_P | LA29_N | HB12_P | HB13_N | TDO | SDA | GND | DP3_C2M_N |
| 32 | HB10_N | GND | LA28_N | GND | HB12_N | GND | 3P3VAUX | GND | DP7_C2M_P | GND |
| 33 | GND | HB15_P | GND | LA31_P | GND | HB19_P | TMS | GND | DP7_C2M_N | GND |
| 34 | HB14_P | HB15_N | LA30_P | LA31_N | HB16_P | HB19_N | TRST_L | GA0 | GND | DP4_C2M_P |
| 35 | HB14_N | GND | LA30_N | GND | HB16_N | GND | GA1 | 12P0V | GND | DP4_C2M_N |
| 36 | GND | HB18_P | GND | LA33_P | GND | HB21_P | 3P3V | GND | DP6_C2M_P | GND |
| 37 | HB17_P_CC | HB18_N | LA32_P | LA33_N | HB20_P | HB21_N | GND | 12P0V | DP6_C2M_N | GND |
| 38 | HB17_N_CC | GND | LA32_N | GND | HB20_N | GND | 3P3V | GND | GND | DP5_C2M_P |
| 39 | GND | VIO_B_M2C | GND | VADJ | GND | VADJ | GND | 3P3V | GND | DP5_C2M_N |
| 40 | VIO_B_M2C | GND | VADJ | GND | VADJ | GND | 3P3V | GND | RES0 | GND |
| | | | LPC Connector | LPC Connector | | | LPC Connector | LPC Connector | | |

Figure 34 - FMC Pin Assignments (HPC)

## 7.3 Power and Reset

The Texas Instruments PTH08T230WAZ POLA DC-DC Converter is used to create the VADJ supply for the FMC Mezzanine Card, set to +2.5V @ 6A, see Figure 32.

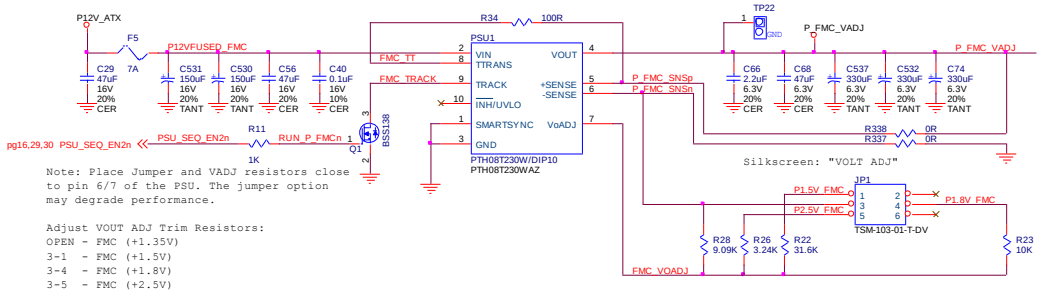



Figure 35 – FMC VADJ Switching Power Supply (+2.5V)

The VADJ voltage can be adjusted by changing the jumper location of JP1;

OPEN - FMC (+1.35V)

Pin 3-1 - FMC (+1.5V)

Pin 3-4 - FMC (+1.8V)

Pin 3-5 - FMC (+2.5V)

Note: FMC Specification allows VADJ -> 0 - 3.3V. VCCO constraints on Virtex-6 devices limits this voltage to 1.14 - 2.625V MAX.

The FMC Specification lists the following recommendations regarding the power pins:

- **12P0V** – These pins carry 12V power from the carrier to the IO Mezzanine module.
- **3P3**V – These pins carry 3.3V power from the carrier to the IO Mezzanine module.
- **3P3VAUX** - A 3.3V auxiliary power supply.
- **VADJ** – These pins carry an adjustable voltage level power from the carrier to the IO Mezzanine module.
- **VREF_A_M2C** – This is the reference voltage associated with the signaling standard used by the bank A data pins, LAxx and HAxx. If the signaling standard on Bank A does not require a reference voltage then this pin can be left unconnected. Note: This option is not supported.

- **VREF_B_M2C** – This is the reference voltage associated with the signaling standard used by the bank B data pins, HBxx. If the signaling standard on Bank B does not require a reference voltage then this pin can be left unconnected. Note: This option is not supported.

- **VIO_B_M2C** – This voltage is generated by the Mezzanine module and is used as the main voltage to power the IO banks on the FPGA that interface to the Bank B IO pins of the connector. Note: This option is not supported.

- **PG_C2M** – Power Good Carrier Card. This signal asserts high by the carrier card when power supplies, VADJ, 12P0V, 3P3V, are within tolerance. Note: This option is not supported, pull-up with resistor.

- **PG_M2C** – Power Good Mezzanine. This signal asserts high by the mezzanine module when power supplies, VIO_B_M2C, VREF_A_M2C, VREF_B_M2C, are within tolerance. Note: This option is not supported pull-up with resistor.

## 7.4 FMC to FPGA IO Connections

Table 39 lists the input/output interconnect between the Virtex-6 FPGA and the FMC Mezzanine Card.

Table 39 – FMC to FPGA IO Connections

| Signal Name | FMC Mezzanine Connector | FPGA |
|---|---|---|
| FMC_CLK0_M2C_P | J8-H4 | U34-AR22 |
| FMC_CLK0_M2C_N | J8-H5 | U34-AR21 |
| FMC_CLK1_M2C_P | J8-G2 | U34-R31 |
| FMC_CLK1_M2C_N | J8-G3 | U34-R32 |
| FMC_CLK2_BIDIR_P | J8-K4 | U34-R28 |
| FMC_CLK2_BIDIR_N | J8-K5 | U34-P29 |
| FMC_CLK3_BIDIR_P | J8-J2 | U34-AL22 |
| FMC_CLK3_BIDIR_N | J8-J3 | U34-AM22 |
| FMC_CLK_DIR | J8-B1 | U34-G34 |
| FMC_HA00_CC_N | J8-F5 | U34-AK27 |
| FMC_HA00_CC_P | J8-F4 | U34-AJ26 |
| FMC_HA01_CC_N | J8-E3 | U34-BA28 |
| FMC_HA01_CC_P | J8-E2 | U34-AY28 |
| FMC_HA02_N | J8-K8 | U34-AP29 |

| Signal Name | FMC Mezzanine Connector | FPGA |
|---|---|---|
| FMC_HA02_P | J8-K7 | U34-AN29 |
| FMC_HA03_N | J8-J7 | U34-AP28 |
| FMC_HA03_P | J8-J6 | U34-AN28 |
| FMC_HA04_N | J8-F8 | U34-AW29 |
| FMC_HA04_P | J8-F7 | U34-AV29 |
| FMC_HA05_N | J8-E7 | U34-AK28 |
| FMC_HA05_P | J8-E6 | U34-AJ28 |
| FMC_HA06_N | J8-K11 | U34-AT28 |
| FMC_HA06_P | J8-K10 | U34-AR28 |
| FMC_HA07_N | J8-J10 | U34-AU29 |
| FMC_HA07_P | J8-J9 | U34-AT29 |
| FMC_HA08_N | J8-F11 | U34-AL28 |
| FMC_HA08_P | J8-F10 | U34-AL27 |
| FMC_HA09_N | J8-E10 | U34-AT27 |
| FMC_HA09_P | J8-E9 | U34-AR27 |
| FMC_HA10_N | J8-K14 | U34-AW28 |
| FMC_HA10_P | J8-K13 | U34-AV28 |
| FMC_HA11_N | J8-J13 | U34-AK26 |
| FMC_HA11_P | J8-J12 | U34-AJ25 |
| FMC_HA12_N | J8-F14 | U34-BB29 |
| FMC_HA12_P | J8-F13 | U34-BA29 |
| FMC_HA13_N | J8-E13 | U34-BD29 |
| FMC_HA13_P | J8-E12 | U34-BC29 |
| FMC_HA14_N | J8-J16 | U34-AN27 |
| FMC_HA14_P | J8-J15 | U34-AM27 |
| FMC_HA15_N | J8-F17 | U34-BC27 |
| FMC_HA15_P | J8-F16 | U34-BB27 |
| FMC_HA16_N | J8-E16 | U34-BA27 |
| FMC_HA16_P | J8-E15 | U34-AY27 |
| FMC_HA17_CC_N | J8-K17 | U34-AV27 |
| FMC_HA17_CC_P | J8-K16 | U34-AU27 |

| Signal Name | FMC Mezzanine Connector | FPGA |
|---|---|---|
| FMC_HA18_N | J8-J19 | U34-AK25 |
| FMC_HA18_P | J8-J18 | U34-AJ24 |
| FMC_HA19_N | J8-F20 | U34-BD28 |
| FMC_HA19_P | J8-F19 | U34-BC28 |
| FMC_HA20_N | J8-E19 | U34-BD20 |
| FMC_HA20_P | J8-E18 | U34-BD21 |
| FMC_HA21_N | J8-K20 | U34-BD19 |
| FMC_HA21_P | J8-K19 | U34-BC19 |
| FMC_HA22_N | J8-J22 | U34-BC21 |
| FMC_HA22_P | J8-J21 | U34-BB21 |
| FMC_HA23_N | J8-K23 | U34-AT22 |
| FMC_HA23_P | J8-K22 | U34-AT23 |
| FMC_HB00_CC_N | J8-K26 | U34-H32 |
| FMC_HB00_CC_P | J8-K25 | U34-J31 |
| FMC_HB01_N | J8-J25 | U34-A32 |
| FMC_HB01_P | J8-J24 | U34-B31 |
| FMC_HB02_N | J8-F23 | U34-A30 |
| FMC_HB02_P | J8-F22 | U34-B30 |
| FMC_HB03_N | J8-E22 | U34-C33 |
| FMC_HB03_P | J8-E21 | U34-C32 |
| FMC_HB04_N | J8-F26 | U34-M31 |
| FMC_HB04_P | J8-F25 | U34-M30 |
| FMC_HB05_N | J8-E25 | U34-D30 |
| FMC_HB05_P | J8-E24 | U34-E30 |
| FMC_HB06_CC_N | J8-K29 | U34-F32 |
| FMC_HB06_CC_P | J8-K28 | U34-G31 |
| FMC_HB07_N | J8-J28 | U34-A33 |
| FMC_HB07_P | J8-J27 | U34-B32 |
| FMC_HB08_N | J8-F29 | U34-M29 |
| FMC_HB08_P | J8-F28 | U34-N29 |
| FMC_HB09_N | J8-E28 | U34-C31 |

| Signal Name | FMC Mezzanine Connector | FPGA |
|---|---|---|
| FMC_HB09_P | J8-E27 | U34-D31 |
| FMC_HB10_N | J8-K32 | U34-M32 |
| FMC_HB10_P | J8-K31 | U34-N31 |
| FMC_HB11_N | J8-J31 | U34-F30 |
| FMC_HB11_P | J8-J30 | U34-G30 |
| FMC_HB12_N | J8-F32 | U34-K31 |
| FMC_HB12_P | J8-F31 | U34-L30 |
| FMC_HB13_N | J8-E31 | U34-P30 |
| FMC_HB13_P | J8-E30 | U34-R30 |
| FMC_HB14_N | J8-K35 | U34-K32 |
| FMC_HB14_P | J8-K34 | U34-L32 |
| FMC_HB15_N | J8-J34 | U34-G32 |
| FMC_HB15_P | J8-J33 | U34-H31 |
| FMC_HB16_N | J8-F35 | U34-T30 |
| FMC_HB16_P | J8-F34 | U34-T29 |
| FMC_HB17_CC_N | J8-K38 | U34-N34 |
| FMC_HB17_CC_P | J8-K37 | U34-N33 |
| FMC_HB18_N | J8-J37 | U34-A35 |
| FMC_HB18_P | J8-J36 | U34-A34 |
| FMC_HB19_N | J8-E34 | U34-B36 |
| FMC_HB19_P | J8-E33 | U34-B35 |
| FMC_HB20_N | J8-F38 | U34-A37 |
| FMC_HB20_P | J8-F37 | U34-B37 |
| FMC_HB21_N | J8-E37 | U34-K33 |
| FMC_HB21_P | J8-E36 | U34-L33 |
| FMC_LA00_CC_N | J8-G7 | U34-BA22 |
| FMC_LA00_CC_P | J8-G6 | U34-AY22 |
| FMC_LA01_CC_N | J8-D9 | U34-BC22 |
| FMC_LA01_CC_P | J8-D8 | U34-BB22 |
| FMC_LA02_N | J8-H8 | U34-BD23 |
| FMC_LA02_P | J8-H7 | U34-BC23 |

| Signal Name | FMC Mezzanine Connector | FPGA |
|---|---|---|
| FMC_LA03_N | J8-G10 | U34-BB19 |
| FMC_LA03_P | J8-G9 | U34-BA19 |
| FMC_LA04_N | J8-H11 | U34-AV22 |
| FMC_LA04_P | J8-H10 | U34-AU22 |
| FMC_LA05_N | J8-D12 | U34-AW19 |
| FMC_LA05_P | J8-D11 | U34-AV19 |
| FMC_LA06_N | J8-C11 | U34-BB20 |
| FMC_LA06_P | J8-C10 | U34-BA20 |
| FMC_LA07_N | J8-H14 | U34-AU20 |
| FMC_LA07_P | J8-H13 | U34-AT20 |
| FMC_LA08_N | J8-G13 | U34-AY20 |
| FMC_LA08_P | J8-G12 | U34-AW20 |
| FMC_LA09_N | J8-D15 | U34-BA23 |
| FMC_LA09_P | J8-D14 | U34-AY23 |
| FMC_LA10_N | J8-C15 | U34-AR23 |
| FMC_LA10_P | J8-C14 | U34-AP23 |
| FMC_LA11_N | J8-H17 | U34-AW23 |
| FMC_LA11_P | J8-H16 | U34-AV23 |
| FMC_LA12_N | J8-G16 | U34-AY21 |
| FMC_LA12_P | J8-G15 | U34-AW21 |
| FMC_LA13_N | J8-D18 | U34-AN22 |
| FMC_LA13_P | J8-D17 | U34-AN23 |
| FMC_LA14_N | J8-C19 | U34-AV21 |
| FMC_LA14_P | J8-C18 | U34-AU21 |
| FMC_LA15_N | J8-H20 | U34-AU25 |
| FMC_LA15_P | J8-H19 | U34-AT25 |
| FMC_LA16_N | J8-G19 | U34-AN26 |
| FMC_LA16_P | J8-G18 | U34-AM26 |
| FMC_LA17_CC_N | J8-D21 | U34-AW24 |
| FMC_LA17_CC_P | J8-D20 | U34-AV24 |
| FMC_LA18_CC_N | J8-C23 | U34-AR26 |

| Signal Name | FMC Mezzanine Connector | FPGA |
|---|---|---|
| FMC_LA18_CC_P | J8-C22 | U34-AP26 |
| FMC_LA19_N | J8-H23 | U34-AY26 |
| FMC_LA19_P | J8-H22 | U34-AW26 |
| FMC_LA20_N | J8-G22 | U34-AK23 |
| FMC_LA20_P | J8-G21 | U34-AJ23 |
| FMC_LA21_N | J8-H26 | U34-BB25 |
| FMC_LA21_P | J8-H25 | U34-BA25 |
| FMC_LA22_N | J8-G25 | U34-AV26 |
| FMC_LA22_P | J8-G24 | U34-AU26 |
| FMC_LA23_N | J8-D24 | U34-AL23 |
| FMC_LA23_P | J8-D23 | U34-AK22 |
| FMC_LA24_N | J8-H29 | U34-AY25 |
| FMC_LA24_P | J8-H28 | U34-AW25 |
| FMC_LA25_N | J8-G28 | U34-BC26 |
| FMC_LA25_P | J8-G27 | U34-BB26 |
| FMC_LA26_N | J8-D27 | U34-AR25 |
| FMC_LA26_P | J8-D26 | U34-AP25 |
| FMC_LA27_N | J8-C27 | U34-AM25 |
| FMC_LA27_P | J8-C26 | U34-AL25 |
| FMC_LA28_N | J8-H32 | U34-BD26 |
| FMC_LA28_P | J8-H31 | U34-BD25 |
| FMC_LA29_N | J8-G31 | U34-AM24 |
| FMC_LA29_P | J8-G30 | U34-AL24 |
| FMC_LA30_N | J8-H35 | U34-BD24 |
| FMC_LA30_P | J8-H34 | U34-BC24 |
| FMC_LA31_N | J8-G34 | U34-AU24 |
| FMC_LA31_P | J8-G33 | U34-AT24 |
| FMC_LA32_N | J8-H38 | U34-AP24 |
| FMC_LA32_P | J8-H37 | U34-AN24 |
| FMC_LA33_N | J8-G37 | U34-BB24 |
| FMC_LA33_P | J8-G36 | U34-BA24 |

| Signal Name | FMC Mezzanine Connector | FPGA |
|---|---|---|
| FMC_PG_C2M | J8-D1 | Pull-Up |
| FMC_PG_M2C | J8-F1 | Pull-Up |
| FMC_PRSNT_M2C_L | J8-H2 | U34-F33 |
| FMC_TX0P | J8-C2 | U34-AN42 |
| FMC_TX0N | J8-C3 | U34-AN41 |
| FMC_RX0P | J8-C6 | U34-AL38 |
| FMC_RX0N | J8-C7 | U34-AL37 |
| FMC_TX1P | J8-A22 | U34-AM44 |
| FMC_TX1N | J8-A23 | U34-AM43 |
| FMC_RX1P | J8-A2 | U34-AM40 |
| FMC_RX1N | J8-A3 | U34-AM39 |
| FMC_TX2P | J8-A26 | U34-AL42 |
| FMC_TX2N | J8-A27 | U34-AL41 |
| FMC_RX2P | J8-A6 | U34-AJ38 |
| FMC_RX2N | J8-A7 | U34-AJ37 |
| FMC_TX3P | J8-A30 | U34-AK44 |
| FMC_TX3N | J8-A31 | U34-AK43 |
| FMC_RX3P | J8-A10 | U34-AK40 |
| FMC_RX3N | J8-A11 | U34-AK39 |
| FMC_TX4P | J8-A34 | U34-AU42 |
| FMC_TX4N | J8-A35 | U34-AU41 |
| FMC_RX4P | J8-A14 | U34-AY40 |
| FMC_RX4N | J8-A15 | U34-AY39 |
| FMC_TX5P | J8-A38 | U34-AT44 |
| FMC_TX5N | J8-A39 | U34-AT43 |
| FMC_RX5P | J8-A18 | U34-AV40 |
| FMC_RX5N | J8-A19 | U34-AV39 |
| FMC_TX6P | J8-B36 | U34-AR42 |
| FMC_TX6N | J8-B37 | U34-AR41 |
| FMC_RX6P | J8-B16 | U34-AT40 |
| FMC_RX6N | J8-B17 | U34-AT39 |

| Signal Name | FMC Mezzanine Connector | FPGA |
|---|---|---|
| FMC_TX7P | J8-B32 | U34-AP44 |
| FMC_TX7N | J8-B33 | U34-AP43 |
| FMC_RX7P | J8-B12 | U34-AP40 |
| FMC_RX7N | J8-B13 | U34-AP39 |
| FMC_TX8P | J8-B28 | U34-BB44 |
| FMC_TX8N | J8-B29 | U34-BB43 |
| FMC_RX8P | J8-B8 | U34-BD40 |
| FMC_RX8N | J8-B9 | U34-BD39 |
| FMC_TX9P | J8-B24 | U34-AY44 |
| FMC_TX9N | J8-B25 | U34-AY43 |
| FMC_RX9P | J8-B4 | U34-BC42 |
| FMC_RX9N | J8-B5 | U34-BC41 |
| FMC_SCL | J8-C30 | U34-G35 |
| FMC_SDA | J8-C31 | U34-F35 |

# 8 MEG-Array Daughter Card Header

The 400 pin MEG-Array connector (P1/P2) is used to interface to Dini Group products, e.g. DNMEG_AD-DA. The daughter card header provides a dedicated global LVDS input clock (from daughter card) connected capable pins on the FPGA and a dedicated global LVDS output clock (input to daughter card). In addition, each IO bank provides a source synchronous LVDS clock that connects to the FPGA. Other connections on the daughter card connector system includes two dedicated, differential clock connections for global clocks, power connections, bank $V_{CCO}$ power, and a reset signal.

## 8.1 Daughter Card clocking

Refer to Daughter Card Header Clocks, par 3.5 in this User Manual.

## 8.2 Daughter Card Header Pin Assignments

The pin assignments of the daughter card header are designed to reduce cross talk to manageable levels while operating at full speed of the Virtex-6 LVDS standards. The daughter card header is divided into five banks, refer to Figure 36. The Virtex-6 devices support source-synchronous interfacing with LVDS signaling at up to 1.6Gbps. The ground-to-signal ratio of the connector is 1:1, refer to Figure 36. General purpose IO is arranged in a GSGS pattern to allow high speed single-ended or differential use. These

signals are routed as loosely-coupled differential signals, meaning when used differentially, they benefit from the noise-resistant properties of a differential pair, but when used in a single-ended configuration, they do not interfere with each other excessively.

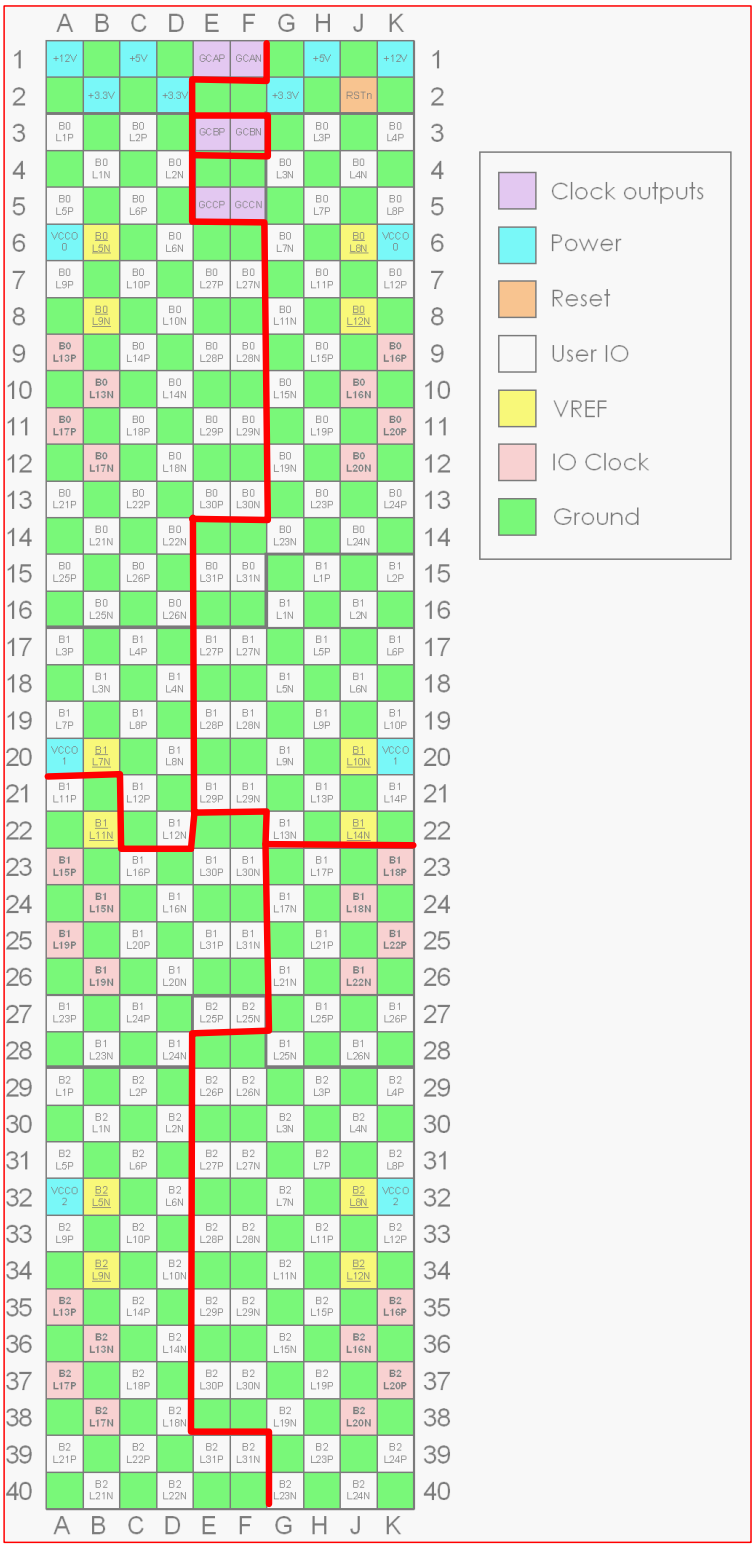



Figure 36 - Daughter Card Header Bank/Pin Assignments

## 8.3 Special Pins on the Daughter Card Header

### 8.3.1 DCA_CLK_DN_IN_P/N, and DCA_CLK_UP_OUT_P/N

The daughter card pin-out defines two bidirectional differential clock pins. These clock signals are intended to be used as differential clock signals. These signals are routed to clock capable (MRCC) inputs on the FPGA and can be used for global clocking.

### 8.3.2 $V_{CCIO}$ Power Supply

On the Virtex-6 FPGA, each IO bank has its own $V_{CCO}$ pins. $V_{CCO}$ is determined by the IO standard for that particular IO bank. Since a daughter card will not always be present on a daughter card connector, a $V_{CCO}$ bias generator is used on the motherboard for each daughter card bank to keep the $V_{CCO}$ pin on the FPGA within its recommended operating range. The Daughter Card drives $V_{CCO}$ to the required level for the particular IO standard. The $V_{CCO}$ impressed by the Daughter Card needs to satisfy the $V_{IH(MAX)}$ of the FPGA on the host board. There are five Adjustable Linear Power Supplies on the board, one per daughter card header IO bank, refer to Figure 37. Refer to the datasheet for the LT1963A from Linear Technology on how to adjust the output voltages. R303 allows the user to remove the powers supply if a $V_{CCO}$ of +2.5V is required, since that voltage can be supplied by the system.

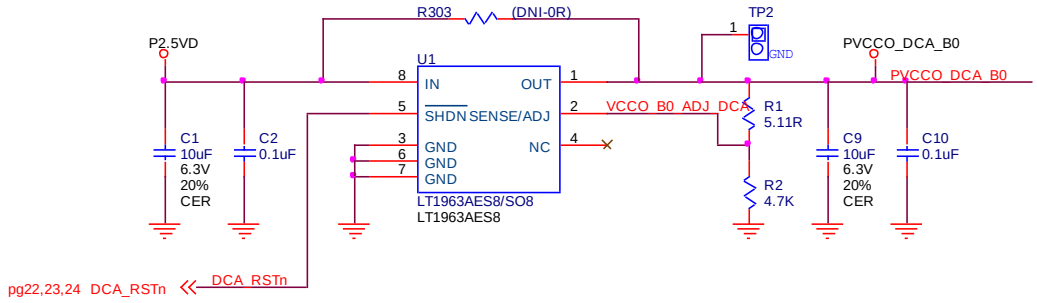



Figure 37 - $V_{CCO}$ Adjustable Linear Power Supply (x5)

## 8.4 Power and Reset

The +12V and +3.3V power rails can be supplied by the daughter card header if the fuses are installed, refer to Figure 38. Each pin on the MEG-Array connector is rated to tolerate 1A of current without thermal overload.

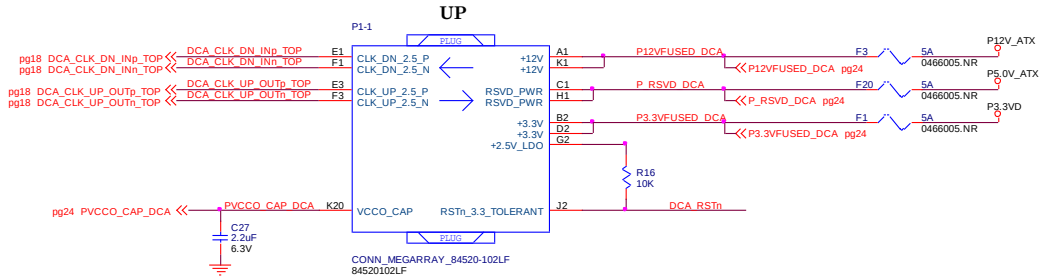



Figure 38 - Daughter Card Header Power & RESET

The "DCA_RSTn" signal is routed from the under voltage reset monitor (U5). The signal is used to hold the $V_{CCO}$ power supplies inactive until the +2.5V supply is stable, in order to meet the Virtex-6 power sequencing requirements, see Table 40.

Table 40 – Daughter VCCO Reset Signal

| Signal Name | OD Buffer | Daughter Card Header |
|---|---|---|
| DCA_RSTn | U5-5 | U12-5, U3-5, U11-5, U1-5, and U2-5 |

## 8.5 FPGA to Daughter Card Header IO Connections

Table 41 lists the input/output interconnect between the Virtex-6 FPGA and the Daughter Card headers on the top/bottom of the board. IO is shared with the exception of the clock inputs/outputs.

Table 41 - FPGA to Daughter Card Header IO Connections

| Signal Name | Daughter Card Receptacle – (TOP) | Daughter Card Plug - (BOTTOM) | FPGA |
|---|---|---|---|
| DCA_CLK_UP_OUTP_TOP | P1-E3 | | U34-P15 |
| DCA_CLK_UP_OUTN_TOP | P1-F3 | | U34-P14 |
| DCA_CLK_DN_INP_TOP | P1-E1 | | U34-J14 |
| DCA_CLK_DN_INN_TOP | P1-F1 | | U34-H13 |
| DCA_CLK_FB_P | U34-AW33 | | U34-AW35 |
| DCA_CLK_FB_N | U34-AY33 | | U34-AY35 |
| DCA_CLK_UP_OUTP_BOT | | P2-E3 | U34-AK35 |
| DCA_CLK_UP_OUTN_BOT | | P2-F3 | U34-AL35 |
| DCA_CLK_DN_INP_BOT | | P2-E1 | U34-AV33 |
| DCA_CLK_DN_INN_BOT | | P2-F1 | U34-AW34 |

| Signal Name | Daughter Card Receptacle – (TOP) | Daughter Card Plug - (BOTTOM) | FPGA |
|---|---|---|---|
| DCA_B0_N0_GCC_DN | P1-B4 | P2-B4 | U34-BC12 |
| DCA_B0_N1_VREF | P1-B6 | P2-B6 | U34-BB17 |
| DCA_B0_N10 | P1-G6 | P2-G6 | U34-AU19 |
| DCA_B0_N11 | P1-G8 | P2-G8 | U34-AW18 |
| DCA_B0_N12 | P1-G10 | P2-G10 | U34-AT18 |
| DCA_B0_N13_CC | P1-G12 | P2-G12 | U34-AU16 |
| DCA_B0_N14 | P1-G14 | P2-G14 | U34-AV17 |
| DCA_B0_N15 | P1-G16 | P2-G16 | U34-AY16 |
| DCA_B0_N16 | P1-G18 | P2-G18 | U34-BD15 |
| DCA_B0_N17 | P1-G20 | P2-G20 | U34-BD16 |
| DCA_B0_N2_VREF | P1-B8 | P2-B8 | U34-BD13 |
| DCA_B0_N3 | P1-B10 | P2-B10 | U34-BC14 |
| DCA_B0_N4_CC | P1-B12 | P2-B12 | U34-BC11 |
| DCA_B0_N5 | P1-B14 | P2-B14 | U34-AR20 |
| DCA_B0_N6 | P1-B16 | P2-B16 | U34-BA18 |
| DCA_B0_N7 | P1-B18 | P2-B18 | U34-BD10 |
| DCA_B0_N8_GCC_BUS | P1-F5 | P2-F5 | U34-BB15 |
| DCA_B0_N9 | P1-G4 | P2-G4 | U34-AP19 |
| DCA_B0_P0_GCC_DN | P1-A3 | P2-A3 | U34-BC13 |
| DCA_B0_P1 | P1-A5 | P2-A5 | U34-BA17 |
| DCA_B0_P10 | P1-H5 | P2-H5 | U34-AT19 |
| DCA_B0_P11 | P1-H7 | P2-H7 | U34-AV18 |
| DCA_B0_P12 | P1-H9 | P2-H9 | U34-AR18 |
| DCA_B0_P13_CC | P1-H11 | P2-H11 | U34-AT17 |
| DCA_B0_P14 | P1-H13 | P2-H13 | U34-AU17 |
| DCA_B0_P15 | P1-H15 | P2-H15 | U34-AY17 |
| DCA_B0_P16 | P1-H17 | P2-H17 | U34-BC16 |
| DCA_B0_P17 | P1-H19 | P2-H19 | U34-BC17 |
| DCA_B0_P2 | P1-A7 | P2-A7 | U34-BD14 |
| DCA_B0_P3 | P1-A9 | P2-A9 | U34-BB14 |

| Signal Name | Daughter Card Receptacle – (TOP) | Daughter Card Plug - (BOTTOM) | FPGA |
|---|---|---|---|
| DCA_B0_P4_CC | P1-A11 | P2-A11 | U34-BB12 |
| DCA_B0_P5 | P1-A13 | P2-A13 | U34-AP21 |
| DCA_B0_P6 | P1-A15 | P2-A15 | U34-AY18 |
| DCA_B0_P7 | P1-A17 | P2-A17 | U34-BD11 |
| DCA_B0_P8_GCC_BUS | P1-E5 | P2-E5 | U34-BB16 |
| DCA_B0_P9 | P1-H3 | P2-H3 | U34-AP20 |
| DCA_B1_N0 | P1-D4 | P2-D4 | U34-AW14 |
| DCA_B1_N1 | P1-D6 | P2-D6 | U34-AM20 |
| DCA_B1_N10_VREF | P1-J6 | P2-J6 | U34-AN17 |
| DCA_B1_N11_VREF | P1-J8 | P2-J8 | U34-AV13 |
| DCA_B1_N12 | P1-J10 | P2-J10 | U34-AK21 |
| DCA_B1_N13_CC | P1-J12 | P2-J12 | U34-AJ19 |
| DCA_B1_N14 | P1-J14 | P2-J14 | U34-AR17 |
| DCA_B1_N15 | P1-J16 | P2-J16 | U34-AY13 |
| DCA_B1_N16 | P1-J18 | P2-J18 | U34-AN19 |
| DCA_B1_N17 | P1-J20 | P2-J20 | U34-BA15 |
| DCA_B1_N18_CC | P1-D22 | P2-D22 | U34-AT15 |
| DCA_B1_N2 | P1-D8 | P2-D8 | U34-BA13 |
| DCA_B1_N3 | P1-D10 | P2-D10 | U34-AP15 |
| DCA_B1_N4_CC | P1-D12 | P2-D12 | U34-AV14 |
| DCA_B1_N5 | P1-D14 | P2-D14 | U34-AR16 |
| DCA_B1_N6 | P1-D16 | P2-D16 | U34-AK18 |
| DCA_B1_N7 | P1-D18 | P2-D18 | U34-AM17 |
| DCA_B1_N8_CC | P1-D20 | P2-D20 | U34-AT13 |
| DCA_B1_N9 | P1-J4 | P2-J4 | U34-AN21 |
| DCA_B1_P0 | P1-C3 | P2-C3 | U34-AW15 |
| DCA_B1_P1 | P1-C5 | P2-C5 | U34-AL20 |
| DCA_B1_P10 | P1-K5 | P2-K5 | U34-AN18 |
| DCA_B1_P11 | P1-K7 | P2-K7 | U34-AU14 |
| DCA_B1_P12 | P1-K9 | P2-K9 | U34-AJ21 |

| Signal Name | Daughter Card Receptacle – (TOP) | Daughter Card Plug - (BOTTOM) | FPGA |
|---|---|---|---|
| DCA_B1_P13_CC | P1-K11 | P2-K11 | U34-AJ20 |
| DCA_B1_P14 | P1-K13 | P2-K13 | U34-AP18 |
| DCA_B1_P15 | P1-K15 | P2-K15 | U34-AW13 |
| DCA_B1_P16 | P1-K17 | P2-K17 | U34-AM19 |
| DCA_B1_P17 | P1-K19 | P2-K19 | U34-AY15 |
| DCA_B1_P18_CC | P1-C21 | P2-C21 | U34-AR15 |
| DCA_B1_P2 | P1-C7 | P2-C7 | U34-BA14 |
| DCA_B1_P3 | P1-C9 | P2-C9 | U34-AN16 |
| DCA_B1_P4_CC | P1-C11 | P2-C11 | U34-AU15 |
| DCA_B1_P5 | P1-C13 | P2-C13 | U34-AP16 |
| DCA_B1_P6 | P1-C15 | P2-C15 | U34-AJ18 |
| DCA_B1_P7 | P1-C17 | P2-C17 | U34-AL18 |
| DCA_B1_P8_CC | P1-C19 | P2-C19 | U34-AT14 |
| DCA_B1_P9 | P1-K3 | P2-K3 | U34-AM21 |
| DCA_B2_N0 | P1-B24 | P2-B24 | U34-AK16 |
| DCA_B2_N1 | P1-B26 | P2-B26 | U34-AR11 |
| DCA_B2_N10 | P1-G26 | P2-G26 | U34-AL15 |
| DCA_B2_N11 | P1-G28 | P2-G28 | U34-AN14 |
| DCA_B2_N12_CC | P1-G30 | P2-G30 | U34-AR12 |
| DCA_B2_N13 | P1-G32 | P2-G32 | U34-AM16 |
| DCA_B2_N14 | P1-G34 | P2-G34 | U34-AU12 |
| DCA_B2_N15 | P1-G36 | P2-G36 | U34-AM14 |
| DCA_B2_N16 | P1-G38 | P2-G38 | U34-AY8 |
| DCA_B2_N17 | P1-G40 | P2-G40 | U34-AY6 |
| DCA_B2_N18_CC | P1-G22 | P2-G22 | U34-AW6 |
| DCA_B2_N2 | P1-B28 | P2-B28 | U34-AW11 |
| DCA_B2_N3_CC | P1-B30 | P2-B30 | U34-AU10 |
| DCA_B2_N4_VREF | P1-B32 | P2-B32 | U34-AV8 |
| DCA_B2_N5_VREF | P1-B34 | P2-B34 | U34-AW10 |
| DCA_B2_N6 | P1-B36 | P2-B36 | U34-AV6 |

| Signal Name | Daughter Card Receptacle – (TOP) | Daughter Card Plug - (BOTTOM) | FPGA |
|---|---|---|---|
| DCA_B2_N7 | P1-B38 | P2-B38 | U34-AN12 |
| DCA_B2_N8_CC | P1-B40 | P2-B40 | U34-AW8 |
| DCA_B2_N9 | P1-G24 | P2-G24 | U34-AJ15 |
| DCA_B2_P0 | P1-A23 | P2-A23 | U34-AK17 |
| DCA_B2_P1 | P1-A25 | P2-A25 | U34-AP11 |
| DCA_B2_P10 | P1-H25 | P2-H25 | U34-AK15 |
| DCA_B2_P11 | P1-H27 | P2-H27 | U34-AM15 |
| DCA_B2_P12_CC | P1-H29 | P2-H29 | U34-AP13 |
| DCA_B2_P13 | P1-H31 | P2-H31 | U34-AL17 |
| DCA_B2_P14 | P1-H33 | P2-H33 | U34-AT12 |
| DCA_B2_P15 | P1-H35 | P2-H35 | U34-AL14 |
| DCA_B2_P16 | P1-H37 | P2-H37 | U34-AW9 |
| DCA_B2_P17 | P1-H39 | P2-H39 | U34-AY7 |
| DCA_B2_P18_CC | P1-H21 | P2-H21 | U34-AV7 |
| DCA_B2_P2 | P1-A27 | P2-A27 | U34-AV12 |
| DCA_B2_P3_CC | P1-A29 | P2-A29 | U34-AU11 |
| DCA_B2_P4 | P1-A31 | P2-A31 | U34-AU9 |
| DCA_B2_P5 | P1-A33 | P2-A33 | U34-AV11 |
| DCA_B2_P6 | P1-A35 | P2-A35 | U34-AU7 |
| DCA_B2_P7 | P1-A37 | P2-A37 | U34-AN13 |
| DCA_B2_P8_CC | P1-A39 | P2-A39 | U34-AV9 |
| DCA_B2_P9 | P1-H23 | P2-H23 | U34-AJ16 |
| DCA_B3_N0 | P1-D24 | P2-D24 | U34-AH12 |
| DCA_B3_N1 | P1-D26 | P2-D26 | U34-AV1 |
| DCA_B3_N10 | P1-J26 | P2-J26 | U34-AL12 |
| DCA_B3_N11 | P1-J28 | P2-J28 | U34-AM11 |
| DCA_B3_N12_CC | P1-J30 | P2-J30 | U34-AT7 |
| DCA_B3_N13_VREF | P1-J32 | P2-J32 | U34-AM10 |
| DCA_B3_N14_VREF | P1-J34 | P2-J34 | U34-AU4 |
| DCA_B3_N15 | P1-J36 | P2-J36 | U34-AW3 |

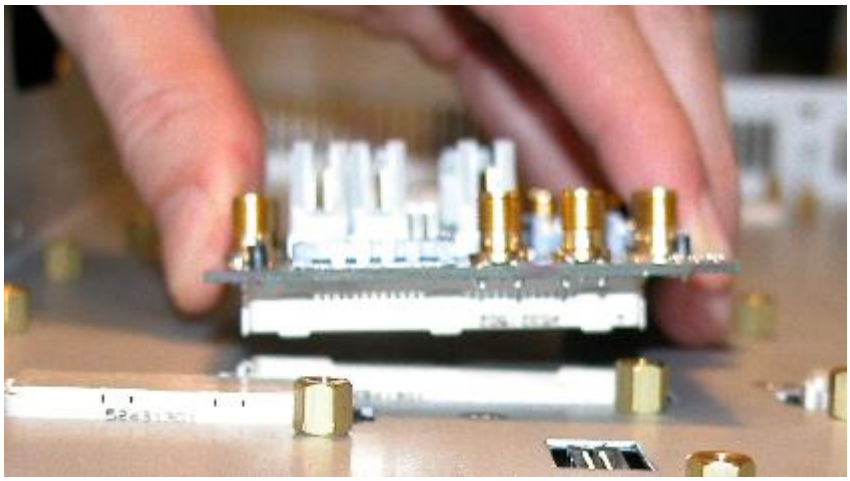
| Signal Name | Daughter Card Receptacle – (TOP) | Daughter Card Plug - (BOTTOM) | FPGA |
|---|---|---|---|
| DCA_B3_N16 | P1-J38 | P2-J38 | U34-AV3 |
| DCA_B3_N17_CC | P1-J40 | P2-J40 | U34-AR6 |
| DCA_B3_N18 | P1-J22 | P2-J22 | U34-AK10 |
| DCA_B3_N2 | P1-D28 | P2-D28 | U34-AK12 |
| DCA_B3_N3_CC | P1-D30 | P2-D30 | U34-AP10 |
| DCA_B3_N4 | P1-D32 | P2-D32 | U34-AT2 |
| DCA_B3_N5 | P1-D34 | P2-D34 | U34-AT4 |
| DCA_B3_N6 | P1-D36 | P2-D36 | U34-AJ13 |
| DCA_B3_N7 | P1-D38 | P2-D38 | U34-AT8 |
| DCA_B3_N8_CC | P1-D40 | P2-D40 | U34-AU5 |
| DCA_B3_N9 | P1-J24 | P2-J24 | U34-AU1 |
| DCA_B3_P0 | P1-C23 | P2-C23 | U34-AH13 |
| DCA_B3_P1 | P1-C25 | P2-C25 | U34-AV2 |
| DCA_B3_P10 | P1-K25 | P2-K25 | U34-AL13 |
| DCA_B3_P11 | P1-K27 | P2-K27 | U34-AM12 |
| DCA_B3_P12_CC | P1-K29 | P2-K29 | U34-AR8 |
| DCA_B3_P13 | P1-K31 | P2-K31 | U34-AL10 |
| DCA_B3_P14 | P1-K33 | P2-K33 | U34-AT5 |
| DCA_B3_P15 | P1-K35 | P2-K35 | U34-AW4 |
| DCA_B3_P16 | P1-K37 | P2-K37 | U34-AV4 |
| DCA_B3_P17_CC | P1-K39 | P2-K39 | U34-AR7 |
| DCA_B3_P18 | P1-K21 | P2-K21 | U34-AK11 |
| DCA_B3_P2 | P1-C27 | P2-C27 | U34-AK13 |
| DCA_B3_P3_CC | P1-C29 | P2-C29 | U34-AN11 |
| DCA_B3_P4 | P1-C31 | P2-C31 | U34-AT3 |
| DCA_B3_P5 | P1-C33 | P2-C33 | U34-AR5 |
| DCA_B3_P6 | P1-C35 | P2-C35 | U34-AJ14 |
| DCA_B3_P7 | P1-C37 | P2-C37 | U34-AT9 |
| DCA_B3_P8_CC | P1-C39 | P2-C39 | U34-AU6 |
| DCA_B3_P9 | P1-K23 | P2-K23 | U34-AU2 |

| Signal Name | Daughter Card Receptacle – (TOP) | Daughter Card Plug - (BOTTOM) | FPGA |
|---|---|---|---|
| DCA_B4_N0 | P1-F7 | P2-F7 | U34-BC9 |
| DCA_B4_N1 | P1-F9 | P2-F9 | U34-BA9 |
| DCA_B4_N10 | P1-F27 | P2-F27 | U34-BA7 |
| DCA_B4_N11_VREF | P1-B20 | P2-B20 | U34-BC2 |
| DCA_B4_N12 | P1-F31 | P2-F31 | U34-BB9 |
| DCA_B4_N13 | P1-F25 | P2-F25 | U34-AY5 |
| DCA_B4_N14 | P1-F35 | P2-F35 | U34-BA2 |
| DCA_B4_N15 | P1-F29 | P2-F29 | U34-BD3 |
| DCA_B4_N16 | P1-F39 | P2-F39 | U34-AY1 |
| DCA_B4_N17 | P1-F33 | P2-F33 | U34-BA3 |
| DCA_B4_N18_CC | P1-F37 | P2-F37 | U34-BB4 |
| DCA_B4_N2 | P1-F11 | P2-F11 | U34-BD4 |
| DCA_B4_N3 | P1-F13 | P2-F13 | U34-BB11 |
| DCA_B4_N4 | P1-F15 | P2-F15 | U34-BB1 |
| DCA_B4_N5 | P1-F17 | P2-F17 | U34-BB6 |
| DCA_B4_N6_CC | P1-F19 | P2-F19 | U34-BD6 |
| DCA_B4_N7_CC | P1-F21 | P2-F21 | U34-BC7 |
| DCA_B4_N8_CC | P1-F23 | P2-F23 | U34-BA4 |
| DCA_B4_N9_VREF | P1-B22 | P2-B22 | U34-AY11 |
| DCA_B4_P0 | P1-E7 | P2-E7 | U34-BB10 |
| DCA_B4_P1 | P1-E9 | P2-E9 | U34-AY10 |
| DCA_B4_P10 | P1-E27 | P2-E27 | U34-BA8 |
| DCA_B4_P11 | P1-A19 | P2-A19 | U34-BC3 |
| DCA_B4_P12 | P1-E31 | P2-E31 | U34-BA10 |
| DCA_B4_P13 | P1-E25 | P2-E25 | U34-AW5 |
| DCA_B4_P14 | P1-E35 | P2-E35 | U34-AY2 |
| DCA_B4_P15 | P1-E29 | P2-E29 | U34-BC4 |
| DCA_B4_P16 | P1-E39 | P2-E39 | U34-AW1 |
| DCA_B4_P17 | P1-E33 | P2-E33 | U34-AY3 |
| DCA_B4_P18_CC | P1-E37 | P2-E37 | U34-BB5 |

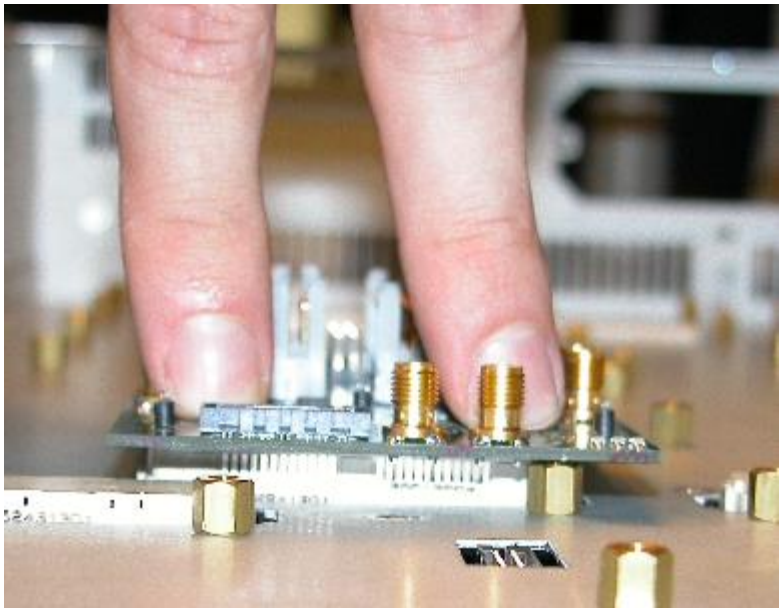
| Signal Name | Daughter Card Receptacle – (TOP) | Daughter Card Plug - (BOTTOM) | FPGA |
|---|---|---|---|
| DCA_B4_P2 | P1-E11 | P2-E11 | U34-BD5 |
| DCA_B4_P3 | P1-E13 | P2-E13 | U34-BA12 |
| DCA_B4_P4 | P1-E15 | P2-E15 | U34-BB2 |
| DCA_B4_P5 | P1-E17 | P2-E17 | U34-BB7 |
| DCA_B4_P6_CC | P1-E19 | P2-E19 | U34-BC6 |
| DCA_B4_P7_CC | P1-E21 | P2-E21 | U34-BC8 |
| DCA_B4_P8_CC | P1-E23 | P2-E23 | U34-BA5 |
| DCA_B4_P9 | P1-A21 | P2-A21 | U34-AY12 |

## 8.6 Insertion/Removal of Daughter Card

Due to the high density MEG-Array connectors, the pins on the plug and receptacle of the MEG-Array connectors are very delicate. When plugging in a daughter card, make sure to align the daughter card first before pressing on the connector. *Be absolutely certain that both the small and the large keys at the narrow ends of the MEG-Array headers line up BEFORE applying pressure to mate the connectors!*



Place it down flat, then press down gently.



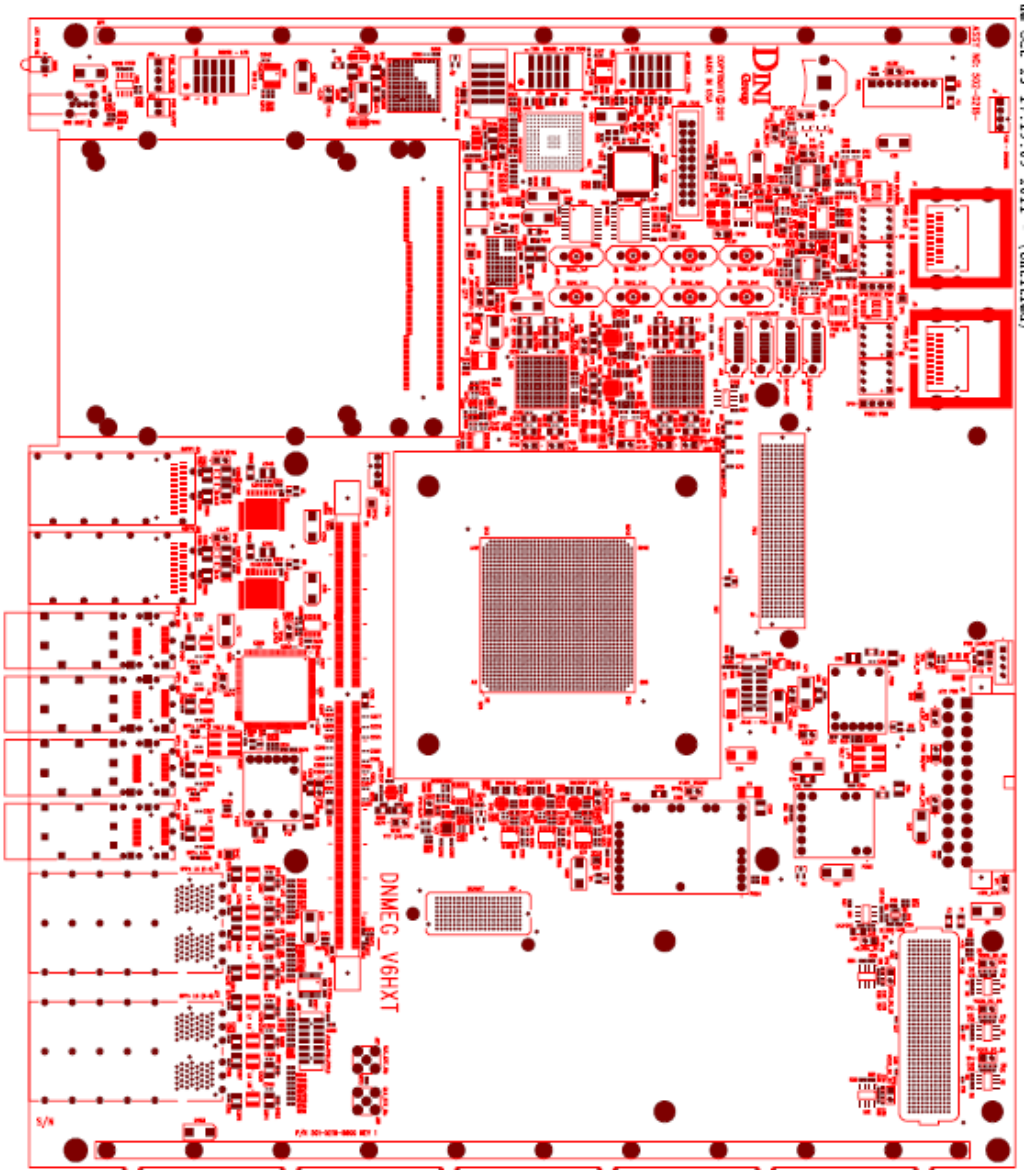
## 8.7 MEG-Array Specifications

| | |
|---|---|
| Manufacturer | FCI |
| Part Number | 74390-101LF – Bottom Receptacle (P2)<br>84520102LF – Top Plug (P1) |
| RoHS Lead Free Compatible | yes |
| Total Number Of Positions | 400 |
| Contact Area Plating | 0.76 µm (30 µin.) gold over 0.76 µm (30 µin.) nickel |
| Mating Force | 30 grams per contact average |
| Unmating Force | 20 grams per contact average |
| Insulation Resistance | 1000 M ohms |
| Withstanding Voltage | 200 VAC |
| Current Rating | 0.45 amps |
| Contact Resistance | 20 to 25 m ohms max (initial), 10 m ohms max increase (after testing) |
| Temperature Range | -40 °C to +85 °C |
| Trademark | MEG-Array® |
| Approvals and Certification | UL and CSA approved |
| Product Specification | GSe -12-100, from FCI websit |
| Pick-up Cap | yes |
| Housing Material | LCP |
| Contact Material | Copper Alloy |
| Durability (Mating Cycles) | 50 |

# 9 Mechanical

## 9.1 Board Dimensions

The DNMEG_V6HXT Logic Emulation Board measures 334mm x 286.5mm. The maximum component height is determined by the FPGA heatsink/fan combo, measured at 70mm. Note: A passive heatsink solution is available for rack mounted applications.

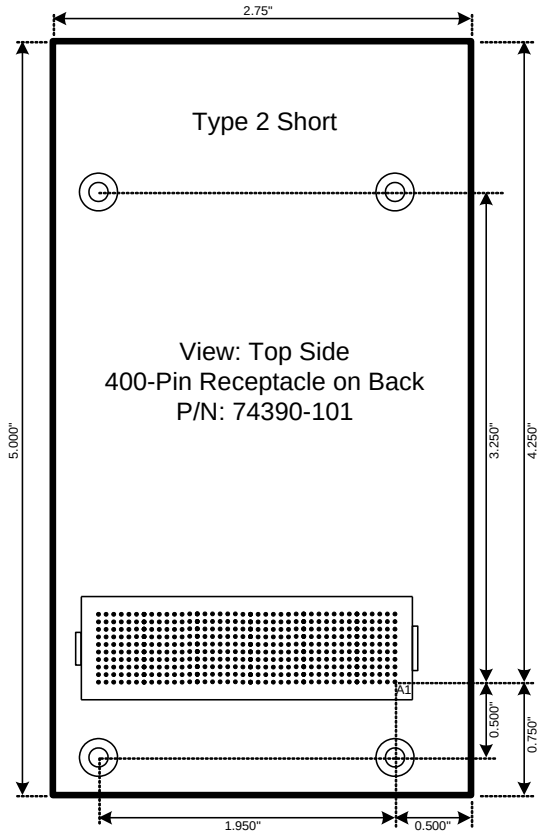



Two bus bars (MP1/MP2) are installed to prevent flexing of the PWB. The mounting holes are connected to the ground plane and can be used to ground test equipment.

Note: Avoid shorting of any power rails or signals to the bus bars - they can conduct a lot of current. Mounting holes are provided to allow the PCB to be mounted in a case or chassis.

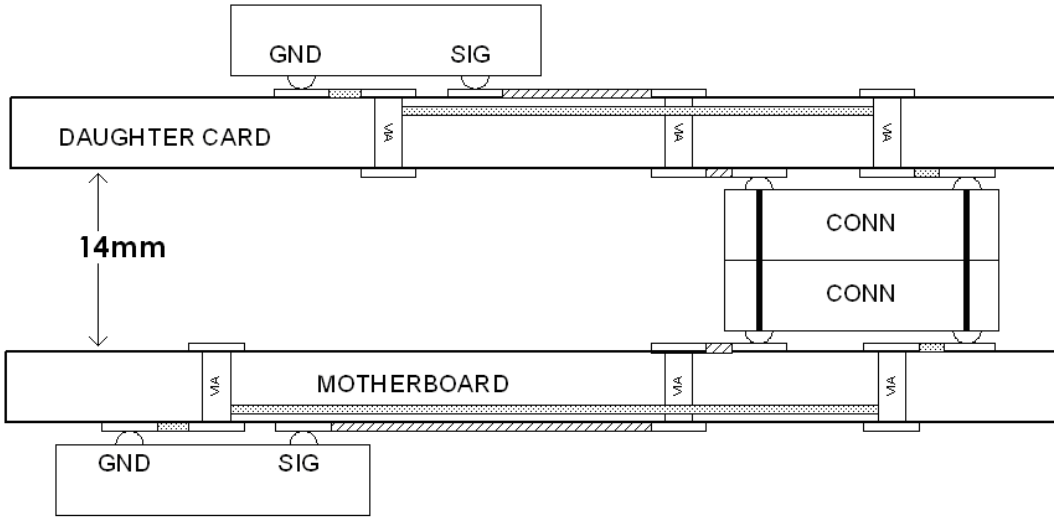
## 9.2 Standard Daughter Card Size

The DNMEG_V6HXT Logic Emulation Board provides mounting hole locations for a Daughter Card with the dimensions given below. The DNMEG_Obs Daughter Card product conforms to these dimensions.




## 9.3 Daughter Card Spacing

With this host-plate-daughter card arrangement, there is a limited Z dimension clearance for backside components on the daughter card. This dimension is determined by the daughter card designer's part selection for the MEG-Array receptacle.




Note that the components on the topside of the daughter card and DNMEG_V6HXT face in opposite directions.

Chapter 5

# Appendix

## 10 Appendix A: UCF File

See the Customer Support Package (USB Flash Drive) for the Xilinx User Constraint Files (UCF) for FPGA.

## 11 Ordering Information

Request quotes by emailing sales@dinigroup.com. For technical questions email support@dinigroup.com